# STUDY OF COMMUTATION FAILURE AND SUBSEQUENT RECOVERY IN HVDC CONVERTERS

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of

MASTER OF TECHNOLOGY

*by*

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*to the*

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INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

MAY, 1988

DEDICATED TO

MY PARENTS

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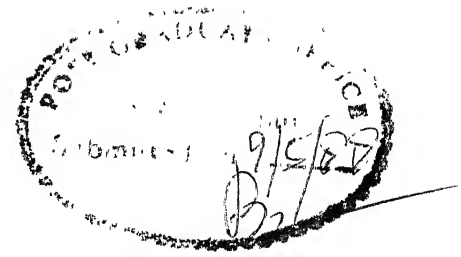

CERTIFICATE

This is to certify that the thesis entitled 'STUDY OF COMMUTATION FAILURE AND SUBSEQUENT RECOVERY IN HVDC CONVERTE submitted by Somesh Kumar in partial fulfilment of the requi ments for the Degree of Master of Technology has been carrie out under my supervision and this has not been submitted elsewhere for a degree.

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Somesh

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# CHAPTER I

# INTRODUCTION

## 1.1 GENERAL

High voltage direct current (HVDC) technology for electrical power transmission has been the focus of attention by power engineers ever since the first commercial DC line was commissioned in 1954. The advantages which it offers vis-a-vis AC transmission for bulk transfer of power, improvement in stability with the presence of a few DC lines in the transmission network provided the initial impetus to pursue this technology. The developments in electronics, in particular power semiconductors, control and power electronics since 1960, further contributed to the rapid growth in the acceptance of HVDC technology the world over. Today there are DC installations of about 20,000 MW already commissioned and about 50,000 MW planned by 1995.

Performance of HVDC systems, however, predominantly depend upon the reliable operation of the converter and its associated control. An effective converter control system should be able to restore the normal operation of the converter at the earliest following a disturbance in the AC or DC networks. The AC system disturbances like single

line to ground faults or 3-phase to ground faults at any remote bus in the AC network or at the bus where the converter is connected (converter AC bus) predominantly effect the converter operation, as these disturbances lead to reduction in the AC phase voltages. The problem is quite severe in case of converter operating in inverter mode. A very frequently encountered problem in inverters is that of commutation failure which occurs mainly due to reduction in the AC phase voltages. For a proper design of converter control system and the associated firing pulse generation scheme, it is necessary to investigate in detail the commutation process in the converter and the various factors which influence it.

## 1.2 COMMUTATION PROCESS

HVDC converters are connected to ac system through converter transformers. The converter valves which start and cease conduction in a sequential manner conduct for a fixed duration. During this period the current flows in a particular phase of the transformer. With the start of conduction of the new valve which is connected to another phase of the transformer the current should transfer to the phase of this incoming valve. Because the transformer and also the AC system behind the transformer has inductance the current in it may vary only at a finite rate. Therefore,

a finite time called the commutation time or overlap period. The process of current transfer during this period is called commutation process. This process is governed by the AC phase voltages, transformer inductance and the magnitude of the DC current [1]. An important criterion in the converter operation is that the commutation process should be completed in a stipulated time which corresponds to the time when the commutation voltage of the incoming and outgoing valve reverses. Failure to meet this criterion leads to the commutation failure in which the successful transfer of the current to the incoming valve does not take place, resulting in the turning off of the incoming valve and the earlier valve continues to conduct. This phenomena occurs mainly when magnitude of AC phase voltage reduces which consequently leads to the shift in the zero crossing of the commutation voltages (line to line voltages) and the increase in the DC link current.

From the point of view of controller design, to take appropriate corrective action, it is therefore necessary to investigate the effect of the disturbance in the AC phase voltage and the instant of its occurrence on commutation process.

## 1.3 CONVERTER RECOVERY FOLLOWING COMMUTATION FAILURE

inverter terminal leads to temporary voltage collapse across the inverter DC terminal due to the conduction of the two valves connected to the same transformer phase [8]. Consequently, current in the DC link increases and although the rectifier being under current control tries to restrict the link current to its rated valve, the time duration of excessive current is substantial, which is hazardous to the system. One way of controlling these overcurrents is to minimise the duration of temporary voltage collapse. In this context several firing strategies are described in [5]. All these various options emphasize on advancing the firing angle of different valves. The paper however does not specify any exact instant to which the firing angle should be advanced. Hence there exists a need to investigate this aspect in detail.

## 1.4 OBJECTIVE AND SCOPE OF THE THESIS

The basic objects of the thesis are :

1) To study in detail the impact of the disturbances in AC phase voltage and the instant of the occurrence of the disturbance on commutation process.
2) To explore the possibility of a specific instant to which the firing of the valve may be advanced so as to improve the recovery process following a commutation

Although it is important to analyse the converter operation with all unbalanced AC voltages, the analysis carried out in the thesis only considers unbalance in a single phase.

## 1.5 OUTLINE OF THE THESIS

A detailed analysis of the inverter operation with a dip in any one of the AC phase voltages has been carried out in Chapter 2. Certain important results regarding the commutation failure have been obtained.

Chapter 3 has been devoted to explain the need of the additional firing requirements to improve the system response following a commutation failure. A scheme is proposed to improve the system response in this context.

Chapter 4 discusses the National HVDC experimental project. Certain cases have been studied on the HVDC system to observe the system recovery response, following a commutation failure, with the scheme proposed in Chapter 3.

The conclusions and scope for further work are presented in Chapter 5.

# CHAPTER 2

# ANALYSIS OF COMMUTATION FAILURE

## 2.1 INTRODUCTION

The valves in the HVDC converters conduct in a specific sequence based on the AC voltages. The transfer of the current from one valve to another called the commutation process depends to a very great extent on the voltage of the AC system connected to the converters. The AC voltages are prone to disturbances and as a result effect the commutation process. Consequently these disturbances may lead to the failure of the completion of the commutation process within a stipulated time. This results in the commutation failure between valves. Particularly in case of inverters, the commutation failure is a very frequent phenomena. Besides this, the behaviour of the inverter following some faults like misfire and quenching etc. is same as that following commutation failure. Thus an understanding of commutation failure and its consequences is important in designing an effective control system to improve converter response following a fault. In this chapter an attempt has been made to analyze the commutation failure in detail including the causes which lead to the commutation failure.

## 2.2 COMMUTATION PROCESS

Commutation process is the phenomena during which an outgoing valve commutates the link current to another incoming valve. The commutation process can be better explained with the help of Fig. 2.1. Fig. 2.1(a) shows AC phase voltage waveforms and Fig. 2.1(b) shows the commutation voltage waveforms for all the 6 valves of a 6 pulse converter shown in Fig. 2.1(c). The commutation voltages as can be seen are the line to line voltages. The necessary conditions for any valve to come into conduction are (i) the voltage across the valve (valve voltage), which under steady state is same as the commutation voltage, must be positive and (ii) the firing pulse for that valve should be present. In case of the inverters, the firing pulse is released for any valve at a firing angle greater than $90^{o}$. This instant is measured with respect to the positive going zero crossing instant of the commutation voltage for that valve. It can be observed in Fig. 2.1(b), that commutation voltage for valve 1 ($e_{ac}$) becomes positive at instant A and assuming a firing angle of $150^{o}$, the firing pulse for valve 1 is released at the instant B. Before instant B, i.e., before valve 1 comes into conduction, there will be valves 5 and 6 conducting in the inverter during steady state. At instant B, valve 1 will come into conduction and the transfer of current

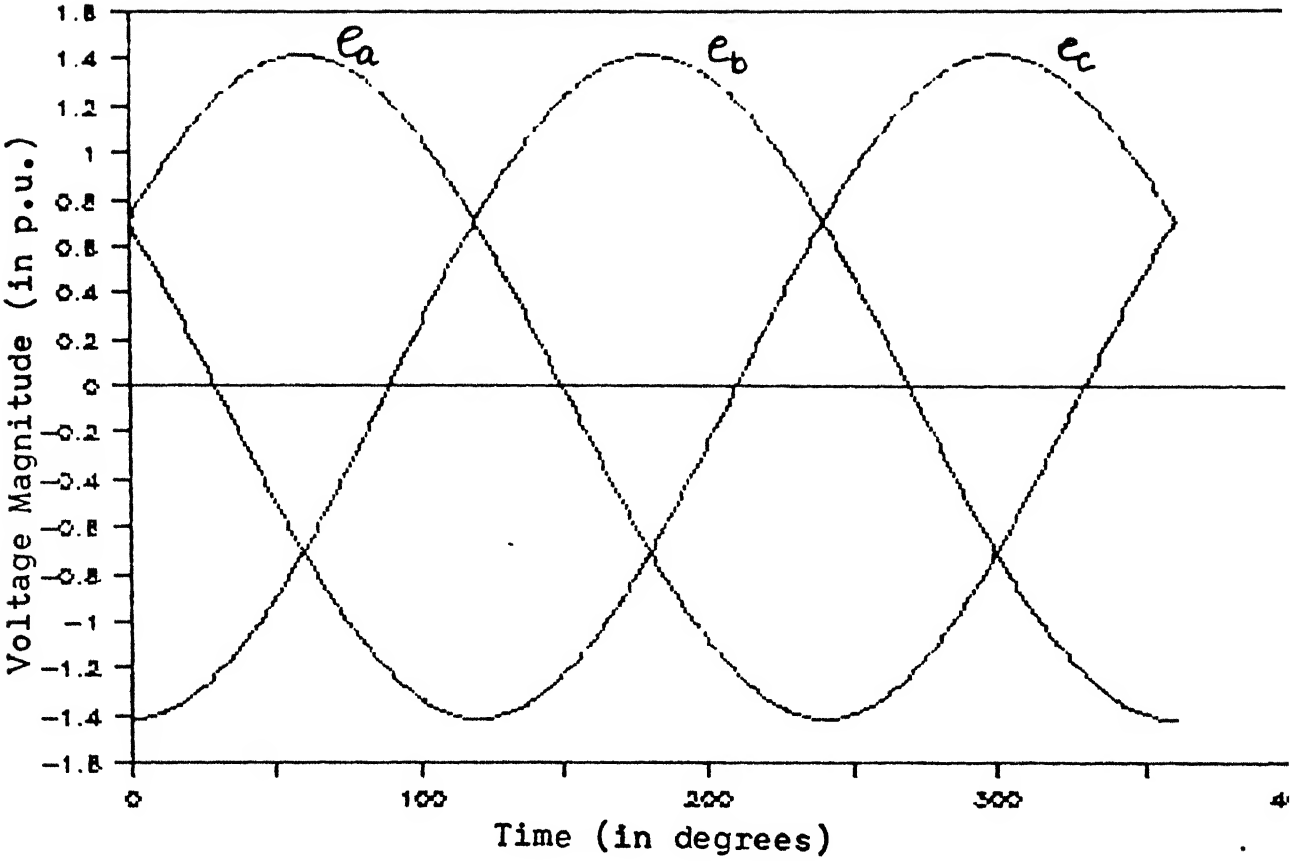
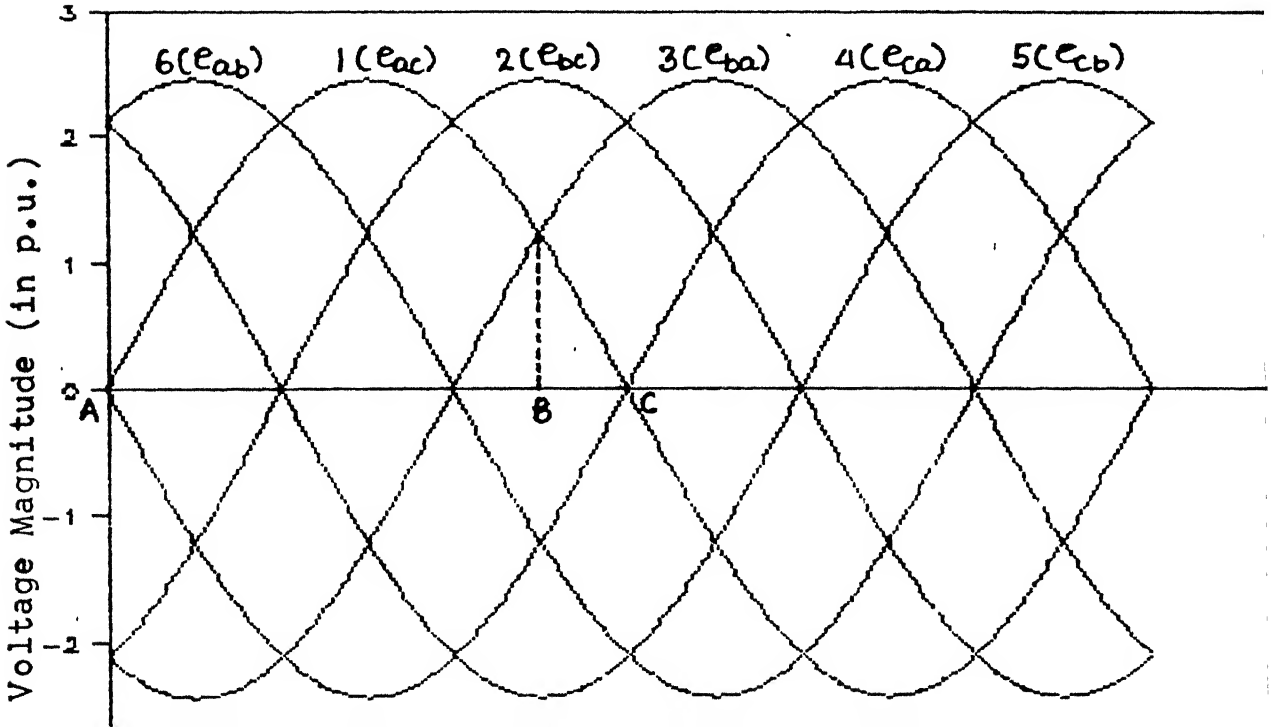



Fig. 2.1(a) A.C. PHASE VOLTAGE WAVEFORMS



current from valve 5 to valve 1 will start. This transition of current will not be instantaneous, but it will be gradual Hence, for a short period of time there will be three valves 5, 6 and 1 conducting. This short period of three valve conduction is known as the overlap period (u). The duration of the overlap period will depend on the rate of change of the valve currents which in turn depend on the magnitude of the commutation voltages and the converter transformer inductance $L_c$. Fig. 2.2 shows the converter circuit under three valve conduction period. $e_a$, $e_b$ and $e_c$ are the AC phase voltages, $L_c$ is the converter transformer inductance and $I_d$ is the d.c. link current.

For the commutation process between incoming valve 1 and the outgoing valve 5, the circuit equation is

$$e_a - L_c \frac{di_1}{dt} + L_c \frac{di_5}{dt} - e_c = 0 \qquad (2.1)$$

where

$$i_1 + i_5 = I_d$$

Assuming DC current to be constant

$$\frac{di_5}{dt} = - \frac{di_1}{dt} \qquad (2.2)$$

substituting eqn. (2.2) in eqn. (2.1) gives

$$\frac{di_1}{dt} = \frac{e_a - e_c}{2L_c} \qquad (2.3)$$

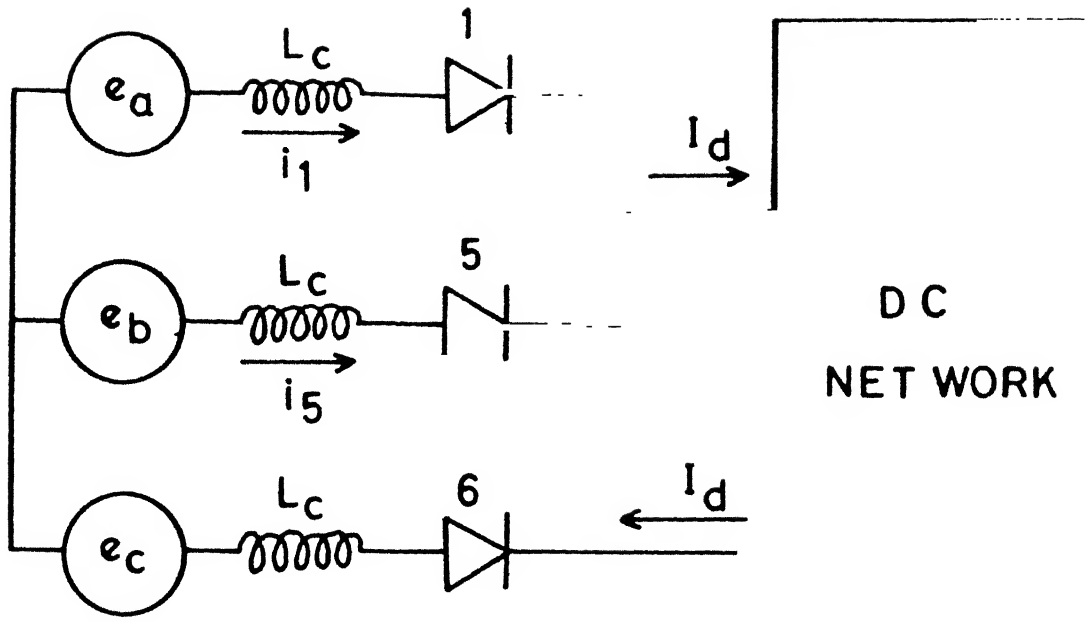



FIG. 2.2 CONVERTER CIRCUIT UNDER THREE VALVE CONDUCTION.

solving the above differential eqn. (2.3), the expression for the average DC current can be obtained as follows.

$$I_d = I_{s2} \left(\frac{\cos \alpha - \cos(\alpha + u)}{2}\right) \qquad (2.4)$$

where

$$I_{s2} = \frac{\sqrt{3}\, E_m}{2\, X_c}$$

It is evident from eqn. (2.3) that rate of change of the valve current will depend on the commutation voltage magnitude. If this commutation process is completed before the instant C (refer Fig. 2.1(b)), then it is a successful commutation and the valve 1 will take over the link current. However, if the commutation process extends beyond point C, then valve 1 will not be able to take up the link current. This is because after the point C, the commutation voltage of valve 1 ($e_{ac}$) becomes negative and that of valve 5 ($e_{ca}$) becomes positive. From (2.3) it is evident that the rate of change of current through valve 1 will be negative as a result the current through valve 1 will start decreasing. Consequently, the rate of change of current of valve 5 will become positive and as a result current through it will start increasing. The decrease in the current through valve 1 will finally lead to the turning off of the valve 1 and valve 5 will continue to conduct. This event, in which a valve which was scheduled to takeover the link current but fails to do so is known as

defined as the failure to commutate before the commutation voltage reverses [1]. It can also be observed in Fig. 2.1(b) that at instant C, the sum of firing angle $\alpha$ and overlap period u is $180^{o}$. Thus it is evident that in case of commutation failure ($\alpha$+u) is greater than $180^{o}$. In case there is no commutation failure then the margin ($180^{o}$ - ($\alpha$+u)) is known as the extinction angle and during steady state operation a minimum value of $\gamma$, known as the $\gamma_c$ is maintained. During this period ($\gamma_c$) the outgoing valve is subjected to reverse bias and is driven deep into turn off to withstand the forward voltage which the valve has to block before coming into conduction again. This necessitates the inverter operation under constant extinction angle control. Fig. 2.3 shows the voltage across a valve in inverter operation during steady state. It can be observed in Fig. 2.3 that valve has to block the positive voltage during the blocking period.

## 2.3 FACTORS LEADING TO COMMUTATION FAILURE

From the above description it is obvious that commutation failure occurs when overlap period exceeds a stipulated margin. The duration of the overlap period depends on the following three factors.

1) The value of the DC current : From (2.4) it can be observed that for a fired valve of $\alpha$, the overlap period

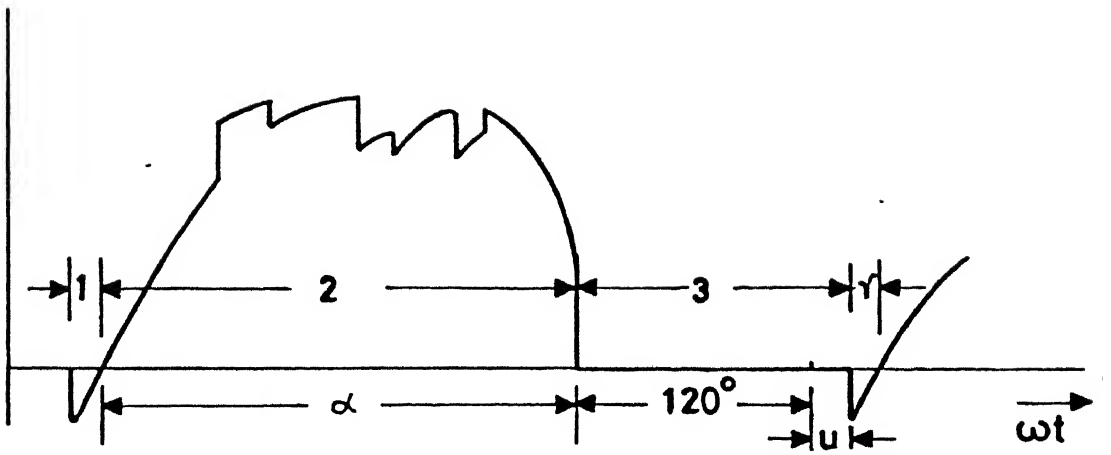



FIG. 2.3 VOLTAGE ACROSS A VALVE IN. inverter

1. inverse period 2. blocking period.
3. conducting period.
$\alpha$. delay or firing angle.
$\gamma$. extinction angle.

2) Value of converter transformer reactance : The rate of change of the valve current is inversely proportional to the value of the converter transformer reactance as can be seen from (2.3). So higher the value of converter transformer reactance, lesser the value of rate of change of valve current and higher will be the duration of the overlap period.

3) Magnitude of the AC phase voltages : It is evident from eqn. (2.3) that the rate of change of valve current in both the valves depends on the magnitude of AC phase voltages and so with a change in the magnitude of the AC phase voltages, the rate of change of the valve current will change and will effect the overlap duration. Besides this, the dip in the AC phase voltages lead to the shifting of the zero crossing of the commutation voltages. This shift in the commutation voltage zero crossing can be in both lead or lag directions. The shift may vary from $0^{\circ}$ to $30^{\circ}$ depending on the magnitude of dip. The relationship between the magnitude of the dip and the magnitude of the shift can be developed with the help of Fig. 2.4(a). Fig. 2.4(a) shows the phasor diagram of the commutation voltages under normal condition and with a dip in phase A. The phase voltages considered are given as follows.

$$e_a = E_m \cos(\omega t - 60)$$

$$e_b = E_m \cos(\omega t - 180)$$

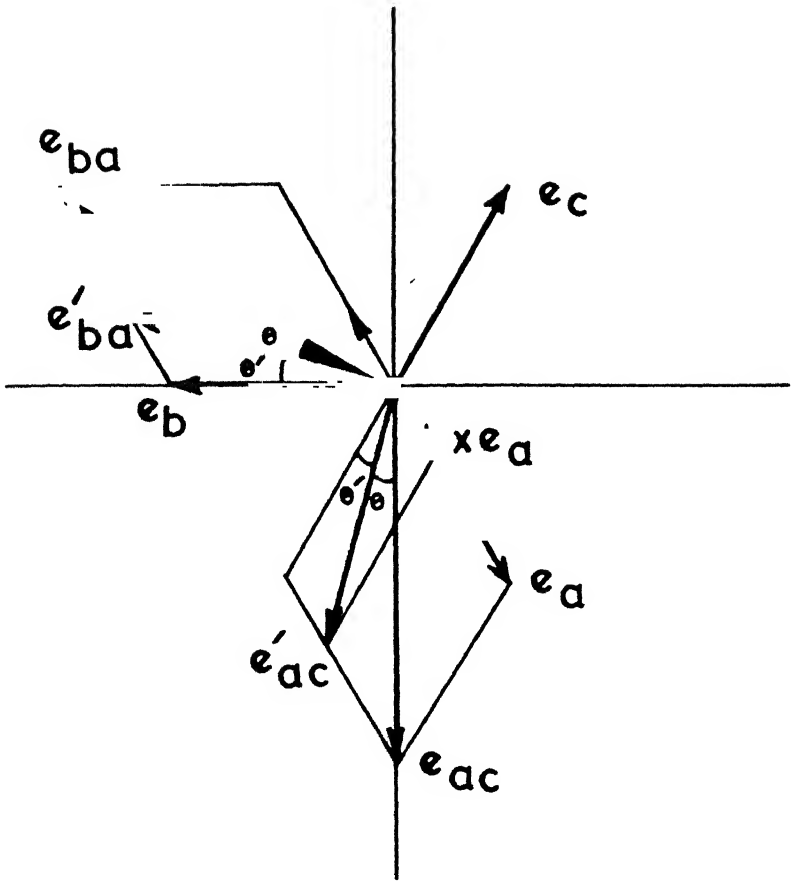



FIG. 2.4 (a) PHASOR DIAGRAM OF THE COMMUTATION VOLTAGE $e_{ac}$ AND $e_{ba}$ UNDER NORMAL CONDITION AND FOLLOWING A DIP IN PHASE

Corresponding commutation voltages for various valves can be obtained as

$$\text{Valve 1} = e_a - e_c = \sqrt{3}\, E_m \sin \omega t$$

$$\text{Valve 3} = e_b - e_a = \sqrt{3}\, E_m \cos(\omega t + 150)$$

$$\text{Valve 5} = e_c - e_b = \sqrt{3}\, E_m \cos(\omega t + 30)$$

$$\text{Valve 4} = e_c - e_a = -\sqrt{3}\, E_m \sin \omega t$$

$$\text{Valve 6} = e_a - e_b = -\sqrt{3}\, E_m \cos(\omega t + 150)$$

$$\text{Valve 2} = e_b - e_c = -\sqrt{3}\, E_m \cos(\omega t + 30)$$

The instant $\omega t = 0$ is defined as the instant when commutation voltage of valve 1 becomes positive.

If a dip of (1-x) p.u. magnitude comes in phase A at instant $\omega t = 0$, then the phase A voltage can be given as

$$e_a = x\, E_m \cos(\omega t - 60)$$

From Fig. 2.4(a) it can be observed that

$e_{ac} = \sqrt{3}\, E_m \sin \omega t$ under normal operation.

$e'_{ac} = K\sqrt{3}\, E_m \sin(\omega t - \theta)$ following a dip in phase A voltage.

$e_{ba} = \sqrt{3}\, E_m \cos(\omega t + 150)$ under normal operation.

$e'_{ba} = \sqrt{3}\, K\, E_m \cos(\omega t + 150 + \theta)$ following a dip in phase A voltage, where K is the factor by which the magnitude of the

commutation voltage changes and $\theta$ is the angle by which the zero crossing of the commutation voltage shifts. To explain the effect of dip in phase voltage, the commutating voltages, under normal condition and following the dip are shown in Figs. 2.4(b). Fig. 2.4(b) shows the shift in zero crossing crossing of the commutation voltages $e_{ba}$ and $e_{ac}$ following a dip in phase A voltage. It can be observed from Fig. 2.4(b) that the zero crossing of the commutation voltage $e_{ac}$ is delayed by an angle $\theta$ (C-C') while the zero crossing of the commutation voltage $e_{ba}$ has advanced by an angle $\theta$(d-d'). In order to calculate the value of $\theta$ in terms of x, it can be assumed that during normal conditions phase voltages have a magnitude of 1 p.u. Hence following the dip, the magnitude of phase A voltage will be X p.u. In Fig. 2.4(a), from parallelogram OABC

$$\tan \theta' = \frac{x \sin 60}{1+x \cos 60} = \frac{\sqrt{3}\, x}{2+x}$$

$$\text{hence } \theta' = \tan^{-1} \frac{\sqrt{3}\, x}{2+x}$$

The value of $\theta$ is given as

$$\theta = 30 - \theta'$$

K can be similarly obtained from parallelogram OABC, as

$$K = \frac{\sqrt{1+x+x^2}}{\sqrt{3}}$$

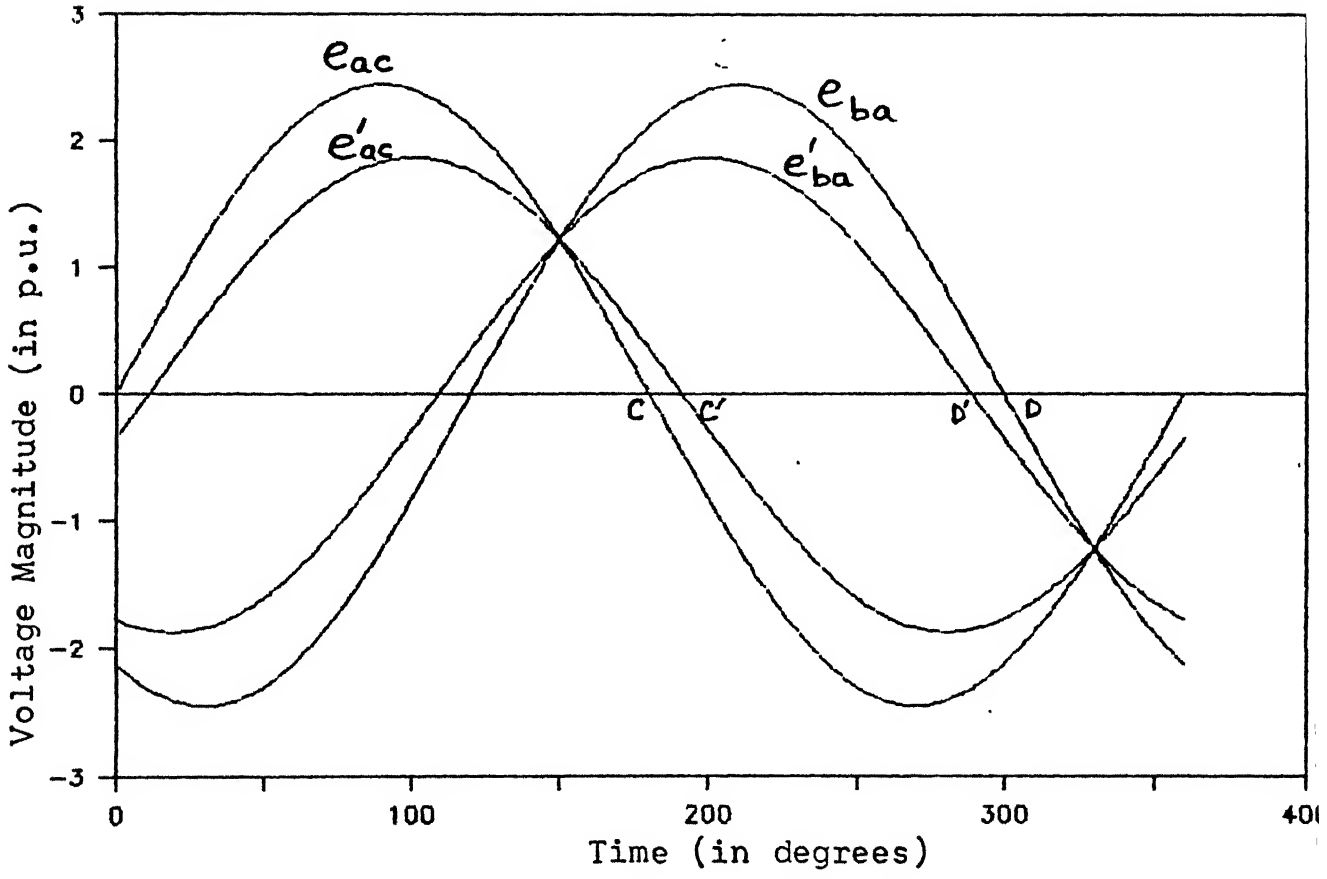



Fig. 2.4(b) WAVEFORM OF COMMUTATION VOLTAGE $e_{ac}$ AND $e_{ba}$ UNDER NORMAL CONDITION AND FOLLOWING A DIP IN PHASE A

This shift in the commutation voltage zero crossing affects the margin required for successful commutation as shown in Figs. 2.5(a) and 2.5(b). Fig. 2.5(a) shows the commutation voltage for valve 1 under normal condition ($e_{ac}$). It is assumed that valve 1 starts conduction at the instant A. Concurrently at this instant, the dip occurs in phase A voltage and as a results, the commutation voltage of valve 1 changes to $e'_{ac}$. Under this condition margin available for successful completion of commutation process between valves 5 and 1 is AC', which under normal condition was AC. It is, therefore, evident that the margin increases thus increasing the time available for completion of commutation process. Similarly Fig. 2.5(b) shows the margin available for completion of commutation process between valves 1 and 3 as a result of dip in phase A voltage which occurs at an instant B concurrent to the firing of valve 3. Beyond instant B the commutation voltage of valve 3 ($e_{ba}$ under normal condition) changes to $e'_{ba}$ following the dip. This leads to a reduced margin BD' (as compared to BD under normal situation) thus increasing the risk of commutation failure. From the above discussion it is evident the change in magnitude of AC phase voltage predominantly affects the commutation process. Thus an analysis of the inverter operation with unbalanced AC voltages is undertaken next.

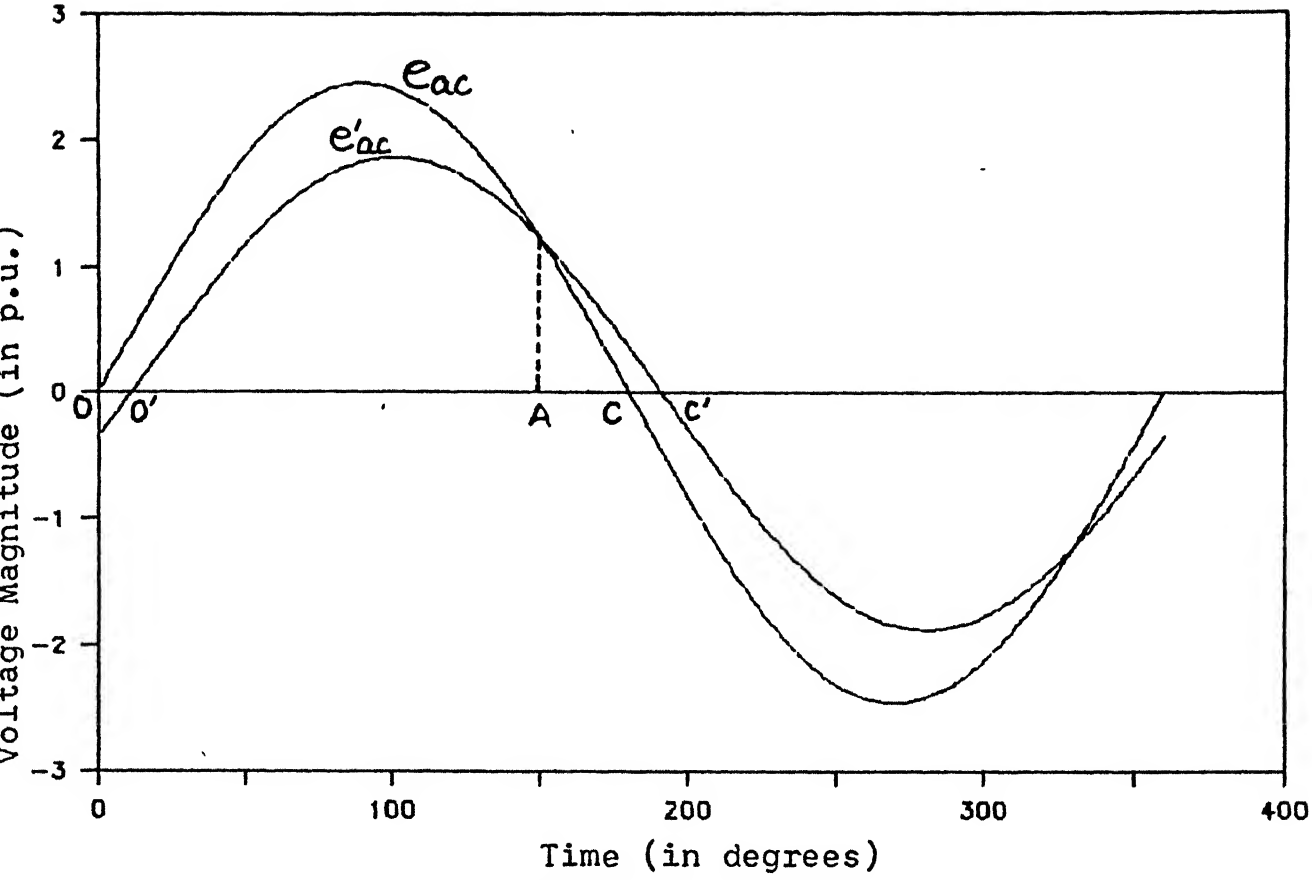
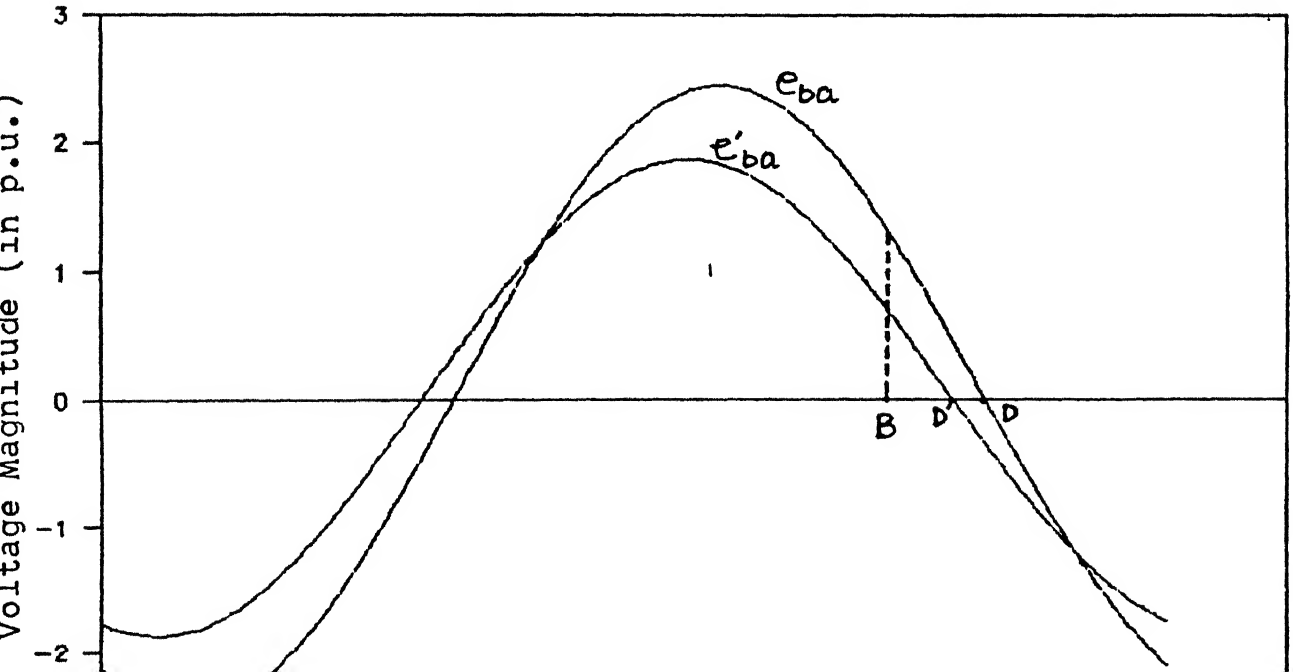



Fig. 2.5(a) COMMUTATION VOLTAGE OF VALVE 1($e_{ac}$)



## 2.4 ANALYSIS OF CONVERTER OPERATION WITH UNBALANCED AC VOLTAGES

Having developed an understanding of how a commutation failure may occur, an analysis has been carried out for a six pulse inverter operation considering a dip in any one of the phases of AC voltages to investigate

i) the effect of the change in the AC voltage magnitude on the commutation process,

ii) the effect of time instant at which the dip occurs.

Following assumptions have been made to simplify the analysis.

i) The DC voltage feeding the inverter terminal is assumed to be constant.

ii) The firing pulses are generated at regular intervals of $60^{o}$ irrespective of the commutation voltage zero crossing and the value of the DC current.

These assumptions, though simplify the analysis represent the worst situation as no control action is being considered based on the value of DC current and AC voltage magnitude. Fig. 2.6 shows the schematic of an inverter terminal fed by a constant DC source $V_{d}$.($e_{a}$, $e_{b}$, $e_{c}$) are the 3-phase AC voltages feeding the converter through a converter transformer having leakage inductance L .

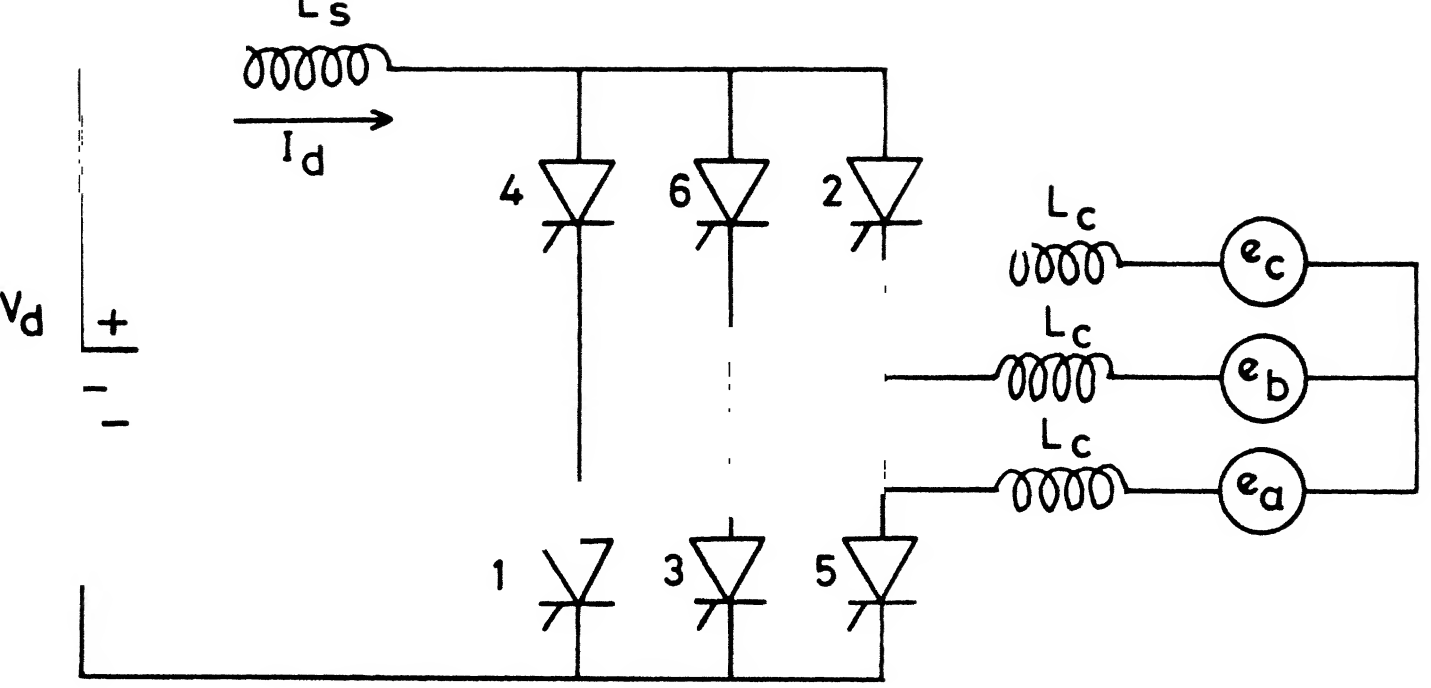



FIG. 2.6 SCHEMATIC OF AN INVERTER TERMINAL FED BY A CONSTANT DC SOURCE.

The dip in phase A is assumed to come at the instant coincident with the firing instant of valve 1 i.e., $\omega t = \alpha$. Initial conditions of operation corresponding to this instant are :

i) Valves 5,6 will be conducting before instant $\omega t = \alpha$.

ii) $I_d$ = normal value of d.c. link current = $I_{do}$.

After valve 1 begins conduction the inverter equivalent circuit is shown in Fig. 2.7. The basic equations for this circuit are :

$$V_p = e_b + L_c \frac{dI_d}{dt} \tag{2.5}$$

$$V_a = xe_a - L_c \frac{di_1}{dt} \tag{2.6}$$

$$V_c = e_c - L_c \frac{di_5}{dt} \tag{2.7}$$

$$V_n = \frac{V_a+V_c}{2} = \frac{e_c - L_c\, di_5/dt + xe_a - L_c\, di_1/dt}{2} \tag{2.8}$$

where $V_p$, $V_n$ are the voltages corresponding to nodes P and n respectively w.r.t. point O. Also

$$V_d - (V_p - V_n) = L_s\, dI_d/dt \tag{2.9}$$

substituting for $V_p$ and $V_n$ from (2.5) and (2.8) in (2.9), the following equation results

$$V_d - e_b + \frac{e_c+xe_a}{2} - \frac{L_c}{2}\frac{di_1}{dt} - \frac{L_c}{2}\frac{di_5}{dt} = (L_s+L_c)\frac{dI_d}{dt} \tag{2.10}$$

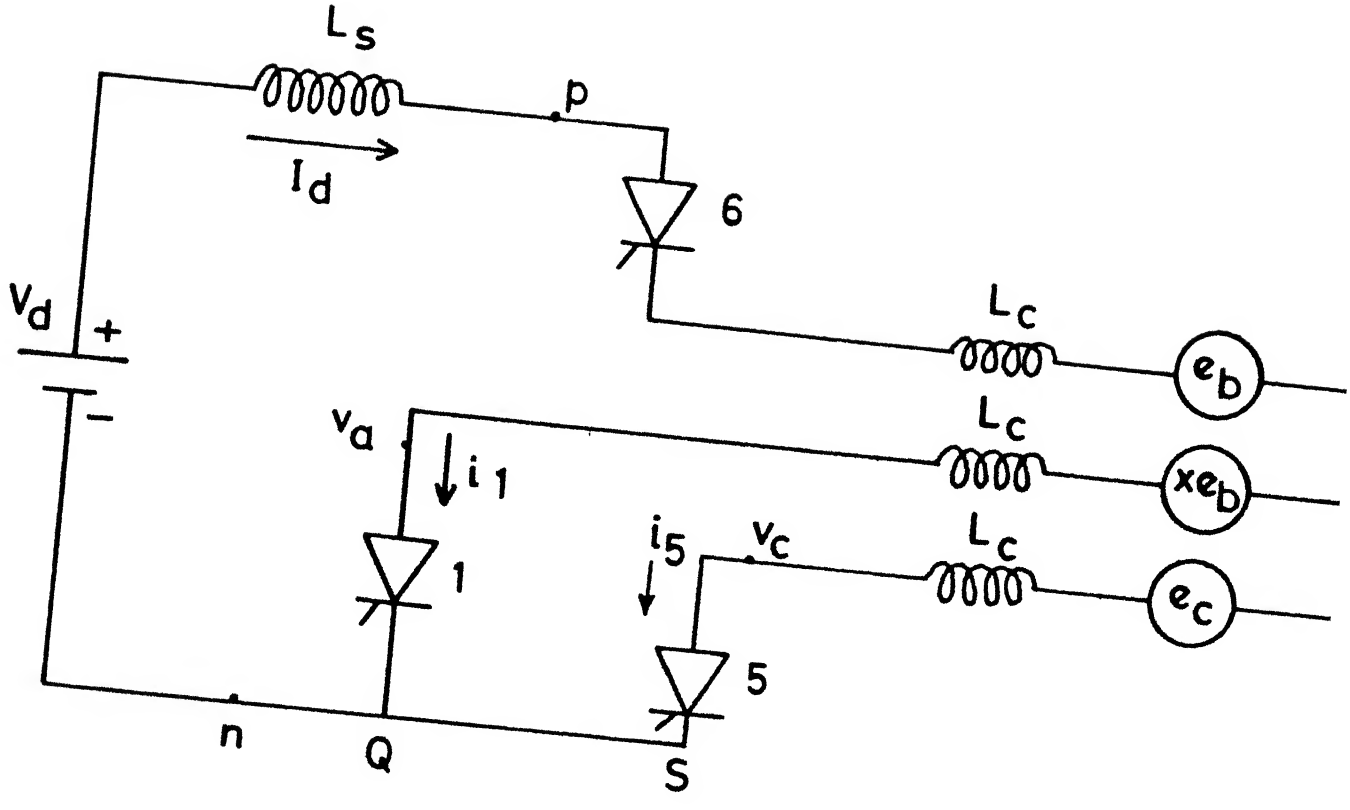



FIG. 2.7 INVERTER EQUIVALENT CIRCUIT FOR 3 VALVE CONDUCTION PERIOD .

In the circuit OQSO it is evident that

$$V_a = V_c \tag{2.11}$$

substituting for $V_a$ and $V_c$ from (2.6) and (2.7) the following equation results

$$L_c \frac{di_1}{dt} = (xe_a - e_c) + L_c \frac{di_5}{dt} \tag{2.12}$$

Also since

$$i_1 + i_5 = I_d \tag{2.13}$$

Therefore,

$$\frac{di_5}{dt} = \frac{dI_d}{dt} - \frac{di_1}{dt} \tag{2.14}$$

substituting (2.14) in (2.12) and simplifying, gives

$$\frac{di_1}{dt} = \frac{1}{2L_c} (xe_a - e_c) + \frac{1}{2} \frac{dI_d}{dt} \tag{2.15}$$

(2.15) gives the rate of change of current of incoming valve. Simplifying the eqn. (2.10) further using (2.14) and (2.15) gives

$$\frac{dI_d}{dt} = \frac{2}{(3L_c+2L_s)} V_d - \frac{2}{(3L_c+2L_s)} \left(e_b - \frac{xe_a+e_c}{2}\right) \tag{2.16}$$

substituting (2.16) in (2.15) gives

$$\frac{di_1}{dt} = \frac{1}{2L_c} (xe_a - e_c) + \frac{V_d}{3L_c+2L_s} - \frac{1}{3L_c+2L_s}$$

Putting the values of $e_a$, $e_b$ and $e_c$ (given in Section 2.3) in (2.17) and simplifying gives

$$\frac{di_1}{d\omega t} = \frac{1}{2X_c}\left[x\,E_m\cos(\omega t-60) - E_m\cos(\omega t+60)\right]$$

$$+\frac{1}{(3X_c+2X_s)}\left[V_d - \left(E_m\cos(\omega t-180) - \frac{x\,E_m\cos(\omega t-60) + E_m\cos(\omega t+60)}{2}\right)\right] \qquad (2.18)$$

The solution of (2.18) can be written as

$$i_1 = K_1 + \int e(\omega t)\,d\omega t \qquad (2.19)$$

where

$$\int e(\omega t)\,d\omega t = \left[\frac{xE_m}{2X_c} + \frac{xE_m}{2(3X_c+2X_s)}\right]\sin(\omega t-60)$$

$$-\left[\frac{E_m}{2X_c} - \frac{E_m}{2(3X_c+2X_s)}\right]\sin(\omega t+60)$$

$$-\frac{E_m}{3X_c+2X_s}\sin(\omega t-180) + \frac{V_d}{(3X_c+2X_s)}\,\omega t \qquad (2.20)$$

Using the initial condition $i_1 = 0$ at $\omega t = \alpha$. (2.19) gives the constant of integration $K_1$ as

$$K_1 = -\left[\frac{xE_m}{2X_c} + \frac{xE_m}{2(3X_c+2X_s)}\right]\sin(\alpha-60)$$

$$+\left[\frac{E_m}{2X_c} - \frac{E_m}{2(3X_c+2X_s)}\right]\sin(\alpha+60)$$

$$+\frac{E_m}{(3X_c+2X_s)}\sin(\alpha-180) - \frac{V_d}{(3X_c+2X_s)}\,\alpha \qquad (2.21)$$

Similarly, substituting the values of $e_a$, $e_b$ and $e_c$ in (2.16), following expression is obtained.

$$\frac{dI_d}{dt} = \frac{2}{(3X_c+2X_s)} V_d - \frac{2}{(3X_c+2X_s)} \left(E_m \cos(\omega t-180) - \frac{x E_m \cos(\omega t-60) + x E_m \cos(\omega t+60)}{2}\right) \quad (2.22)$$

The solution of (2.22) is of the form

$$I_d = K_2 + \int p(\omega t)\, d\omega t \quad (2.23)$$

where

$$\int p(\omega t)\, d\omega t = \frac{2V_d}{(3X_c+2X_s)} \omega t - \frac{2E_m}{(3X_c+2X_s)} \sin(\omega t-180) + \frac{xE_m}{(3X_c+2X_s)} \sin(\omega t-60) + \frac{xE_m}{3X_c+2X_s} \sin(\omega t + 60) \quad (2.24)$$

and corresponding to initial conditions $I_d = I_{do}$ at $\omega t = \alpha$, the constant of integration $K_2$ is

$$K_2 = I_{do} - \frac{2V_d}{(3X_c+2X_s)} \alpha + \frac{2 E_m}{3X_c+2X_s} \sin(\alpha-180) - \frac{xE_m}{(3X_c+2X_s)} \sin(\alpha-60) - \frac{E_m}{3X_c+2X_s} \sin(\alpha+60) \quad (2.25)$$

substituting (2.24) and (2.25) in (2.23) gives the value of DC current as a function of $\omega t$.

In order to check for the commutation failure, it has to be checked, whether the current of incoming valve governed by eqn. (2.19) is able to reach upto the value of DC current governed by (2.23) in a stipulated margin or not. If it is able to do so, then it will be a successful commutation with the incoming valve carrying the full DC current and the current of the outgoing valve going to zero thus turning it off. Else, there will be a commutation failure and the outgoing valve will keep on conducting and therefore affecting the normal conduction sequence of valves. The margin available for this commutation process is more as compared to the normal operation (refer Fig. 2.5(a)).

If there is no commutation failure, then at instant $\omega t = \delta = \alpha+u$, the incoming valve current will be equal to the DC current hence

$$I_d/\omega t = \delta \; - i_1/\omega t = \delta \; = 0 \qquad (2.26)$$

Substituting the values of $I_d$ and $i_1$ corresponding to $\omega t = \delta$ from (2.23) and (2.19) in (2.26) gives

$$I_{do} - \frac{2V_d \alpha}{(3X_c+2X_s)} + \frac{2E_m}{(3X_c+2X_s)} \sin(\alpha - 180)$$

$$- \frac{xE_m}{(3X_c+2X_s)} \sin(\alpha-60) - \frac{E_m}{(3X_c+2X_s)} \sin(\alpha+60)$$

$$+ \frac{2V_d}{(3X_c+2X_s)} \delta - \frac{2E_m}{(3X_c+2X_s)} \sin(\delta -180) + \frac{xE_m}{(3X_c+2X_s)}$$

$$\sin(\delta-60) + \frac{E_m}{(3X_c+2X_s)} \sin(\delta+60) + [\frac{x\,E_m}{2\,X_c} + \frac{x\,E_m}{2(3X_c+2X_s)}]$$

$$\sin(\alpha-60) - [\frac{E_m}{2X_c} - \frac{E_m}{2(3X_c+2X_s)}] \sin(\alpha+60) -$$

$$\frac{E_m}{(3X_c+2X_s)} \sin(\alpha-180) + \frac{V_d\ \alpha}{(3X_c+2X_s)} -$$

$$[\frac{x\,E_m}{2X_c} + \frac{x\,E_m}{2(3X_c+2X_s)}] \sin(\delta-60) +$$

$$[\frac{E_m}{2X_c} - \frac{E_m}{2(3X_c+2X_s)}] \sin(\delta+60) +$$

$$\frac{E_m}{(3X_c+2X_s)} \sin(\delta-180) - \frac{Vd}{(3X_c+2X_s)} \delta = 0 \qquad (2.27)$$

The solution of above transcedental equation can be obtained using Newton method [2] and the value of $\delta$ can be obtained. The conduction status will change at instant $\omega t = \delta$ and there will be two valves conducting which in the present case are 6 and 1. The value of DC current can be found out at instant $\omega t = \delta$ From (2.23). the inverter equivalent circuit corresponding to 6 and 1 conduction status is shown in Fig. 2.8.

Following circuit equations can be written for the equivalent circuit

$$v_p = e_b + L_c \frac{dI_d}{dt} \qquad (2.28)$$

$$L \frac{dI_d}{dt}$$

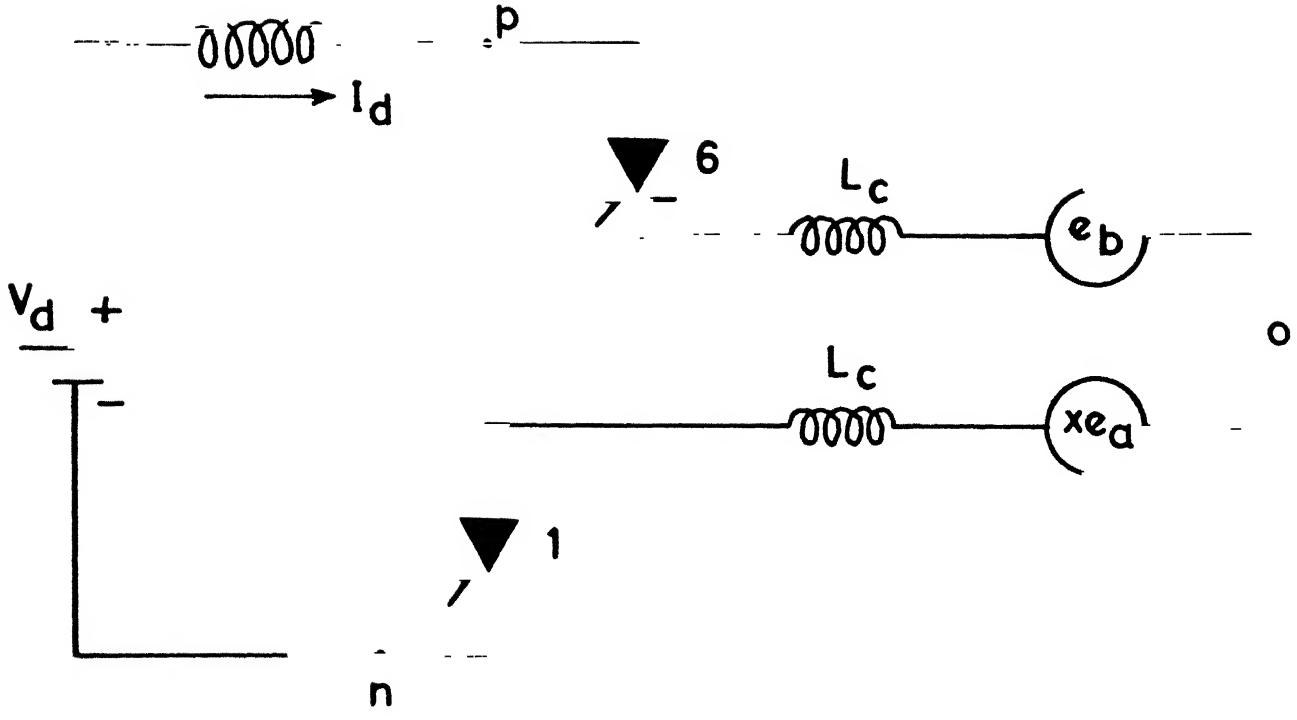



FIG. 2.8 INVERTER EQUIVALENT CIRCUIT FOR 2 VALVE CONDUCTION .

substituting the values of $v_p$ and $v_n$ from (2.28) and (2.29) in (2.30) and further modifying gives

$$\frac{dI_d}{dt} = \frac{v_d}{X_s+2X_c} - \frac{1}{(2X_c+X_s)} [E_m \cos(\omega t - 180)$$

$$- x\ E_m \cos(\omega t - 60)] \qquad (2.31)$$

The solution of the above differential equation is of the form

$$I_d = K_3 + \int e(\omega t)\ d\omega t \qquad (2.32)$$

where $\int e(\omega t)\ d\omega t = \frac{v_d}{(X_s+2X_c)}\ \omega t -$

$$\frac{E_m}{(X_s+2X_c)} \sin(\omega t - 180) + \frac{xE_m}{(X_s+2X_c)} \sin(\omega t - 60) \qquad (2.33)$$

Since $I_d = I_{dl}$ at $\omega t = \delta$ , where $I_{dl}$ is obtained from eqn. (2.23) corresponding to $\omega t = \delta$ , the value of $K_3$ is

$$K_3 = I_{dl} - \frac{v_d}{(X_s+2X_c)}\ \delta + \frac{E_m}{(X_s+2X_c)} \sin$$

$$(\delta - 180) - \frac{xE_m}{(X_s+2X_c)} \sin(\delta - 60) \qquad (2.34)$$

Combining equations (2.32) to (2.34), the value of $I_d$ can be obtained as a function of time. This resulting expression for $I_d$ will hold good over the entire two valve conduction period

till the next valve is fired, which with the considered assumption, will be fired at the instant $\omega t = 60 + \alpha$. The value of $I_d$ at instant $\omega t = \alpha + 60$ can be obtained from (2.32) and this value will be used as an initial condition for the next three valve conduction period. This process is repeated over the complete cycle to calculate the valve current and dc current under 2 and 3 valve conduction mode.

## 2.5 RESULTS

Based on the analyses described in the previous section, an investigation of the commutation process in case of a 6-pulse inverter has been carried out to study the influence of the change in the AC voltage magnitude as well as the instant of its occurrence. The operating conditions and parameters of the 6-pulse inverter system are given in Appendix A.

### 2.5.1 Effect of Dip in AC Phase Voltage Magnitude

As mentioned earlier the process of commutation is greatly influenced by variation in AC phase voltage magnitude. It may therefore be interesting to determine or estimate the critical level of voltage dip which may adversely effect the commutation process and may lead to commutation failure. In this context, several case studies have been carried out considering the dip in different phases of AC voltage, having different

magnitude but occurring at the same instant $\omega t = 0$. The observations are recorded in Table 1.

In all these cases the commutation failure has been detected by observing whether the current of the incoming valve has been able to reach upto the value of the DC current or not in the stipulated time (before the commutation voltage of the valves involved in the commutation process reverses). The variation of the incoming valve current ($i_j$ for valve j) and DC current, for all the cases reported in Table 1 is shown in Figs. 2.9(a) to 2.9(i). Based on the analysis of the previous sections the incoming valve current and the DC current are calculated only upto the instant when the commutation failure occurs. For all the figures the various conducting valves in different regions of time are also given in Table 1.

Fig. 2.9(a) depicts successful commutation between all the valves over the cycle following a 5% dip in phase A AC voltage. It can be seen that because of the dip the DC current is also increasing gradually as expected without hampering the commutation process.

From the cases 2 and 3 reported in Table 1 (Fig. 2.9(b), 2.9(c)) it can be seen that when the dip occurs in phase A then commutation failure occurs during commutation process

Table 1 Effect of magnitude of dip on commutation process

| Phase of dip | Magnitude of dip | Valves conducting in the region | | | | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | OA | AB | BC | CD | DE | EF | FG | GH | HI | IJ | JK | KL | |
| A | 5% | 34 | 345 | 45 | 456 | 56 | 561 | 16 | 612 | 12 | 123 | 23 | 234 | No commutation failure |
| A | 10% | 34 | 345 | 45 | 456 | | | | | | | | | Commutation failure between valves 4 and 6 |
| A | 7% | 34 | 345 | 45 | 456 | 56 | 561 | 61 | 612 | 12 | 123 | | | Commutation failure between valves 1 and 3 |
| B | 15% | 34 | 345 | | | | | | | | | | | Commutation failure between valves 3 and 5 |
| B | 7% | 34 | 345 | 45 | 456 | 56 | 561 | 61 | 612 | | | | | Commutation failure between valves 6 and 2 |
| B | 10% | 34 | 345 | | | | | | | | | | | Commutation failure between valves 3 and 5 |
| C | 10% | 34 | 345 | 45 | 456 | 56 | 561 | | | | | | | Commutation failure between valves 5 and 1 |
| C | 7% | 34 | 345 | 45 | 456 | 56 | 561 | 61 | 612 | 12 | 123 | 23 | 234 | Commutation failure between valves 2 and 4 |
| C | 15% | 34 | 345 | 45 | 456 | 56 | 561 | | | | | | | Commutation failure between valves 5 and 1 |

ll these cases the dip is assumed to come at instant $\omega t = 0$

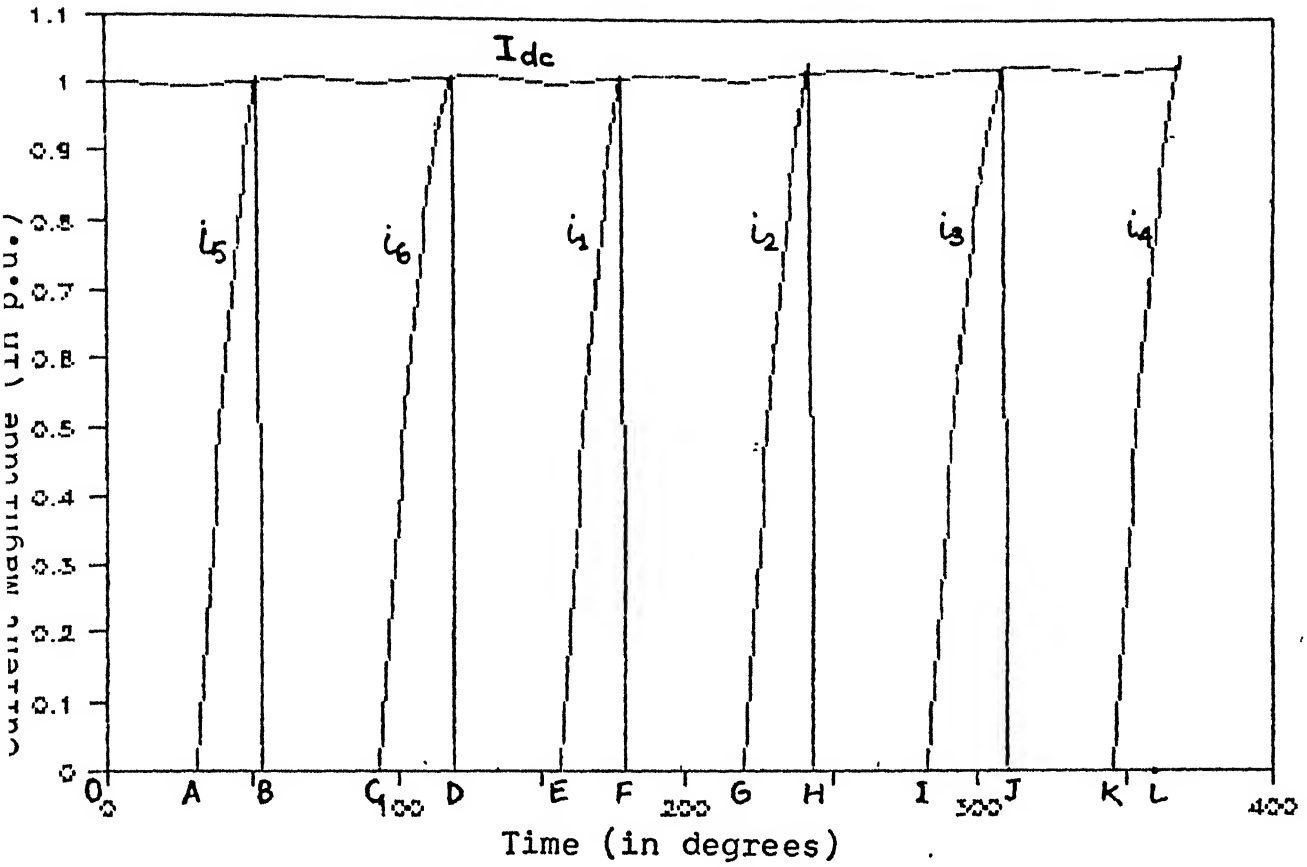
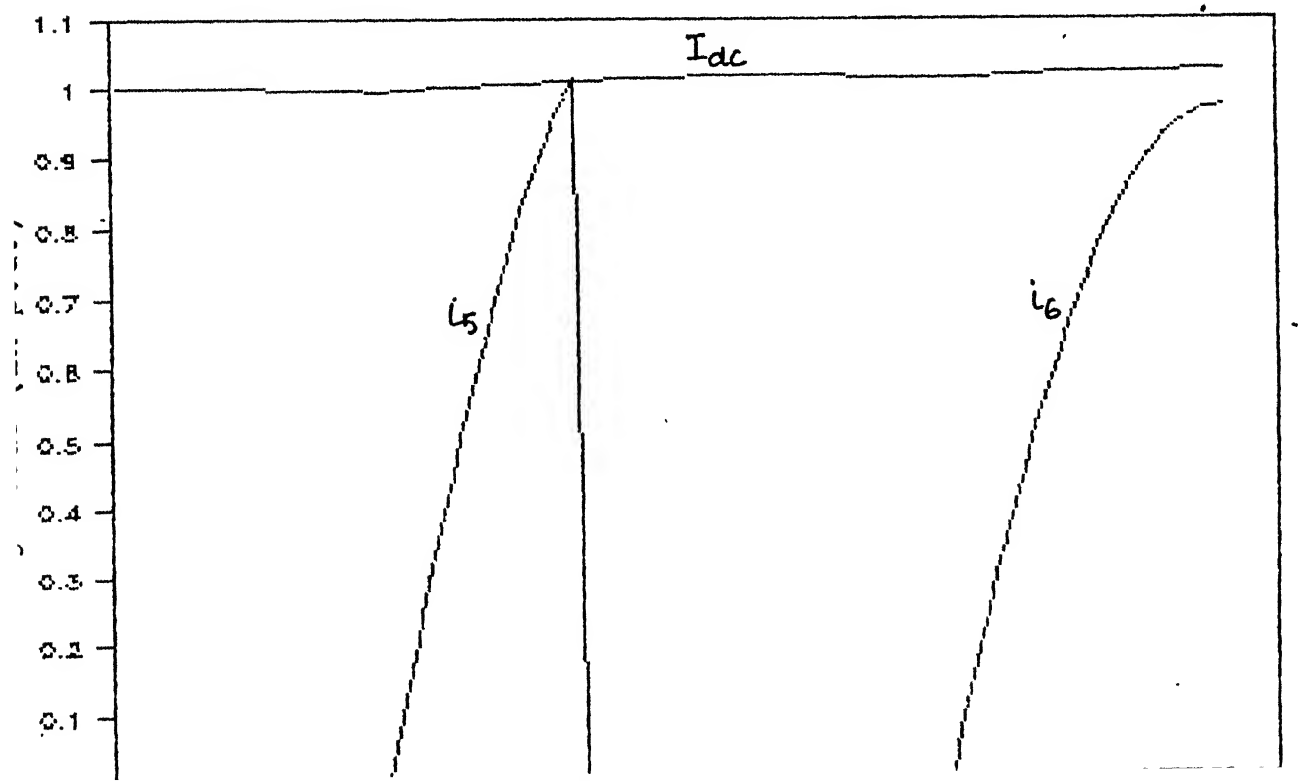



Fig. 2.9(a) INCOMING VALVE CURRENT AND D.C. CURRENT FOR CASE 1 of TABLE 1



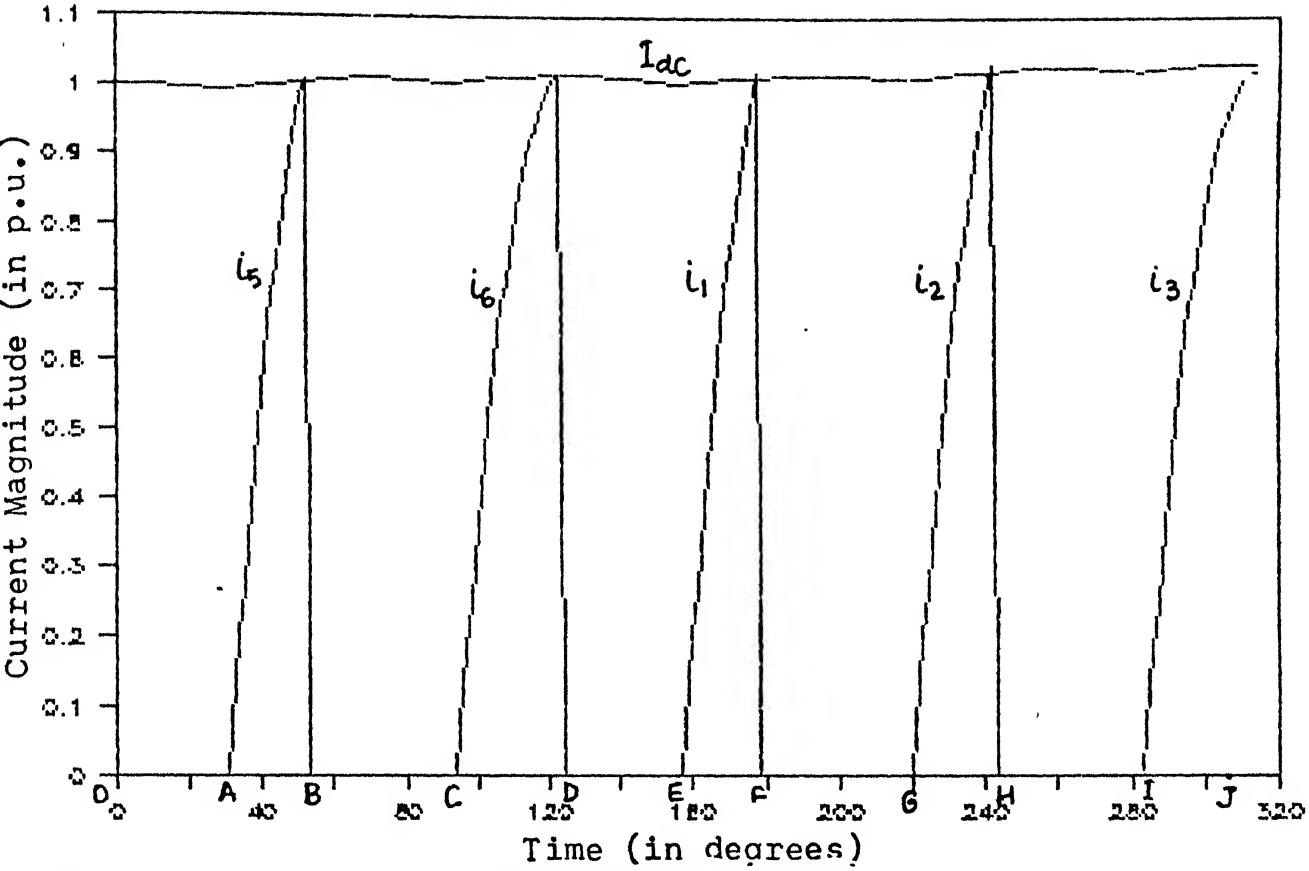
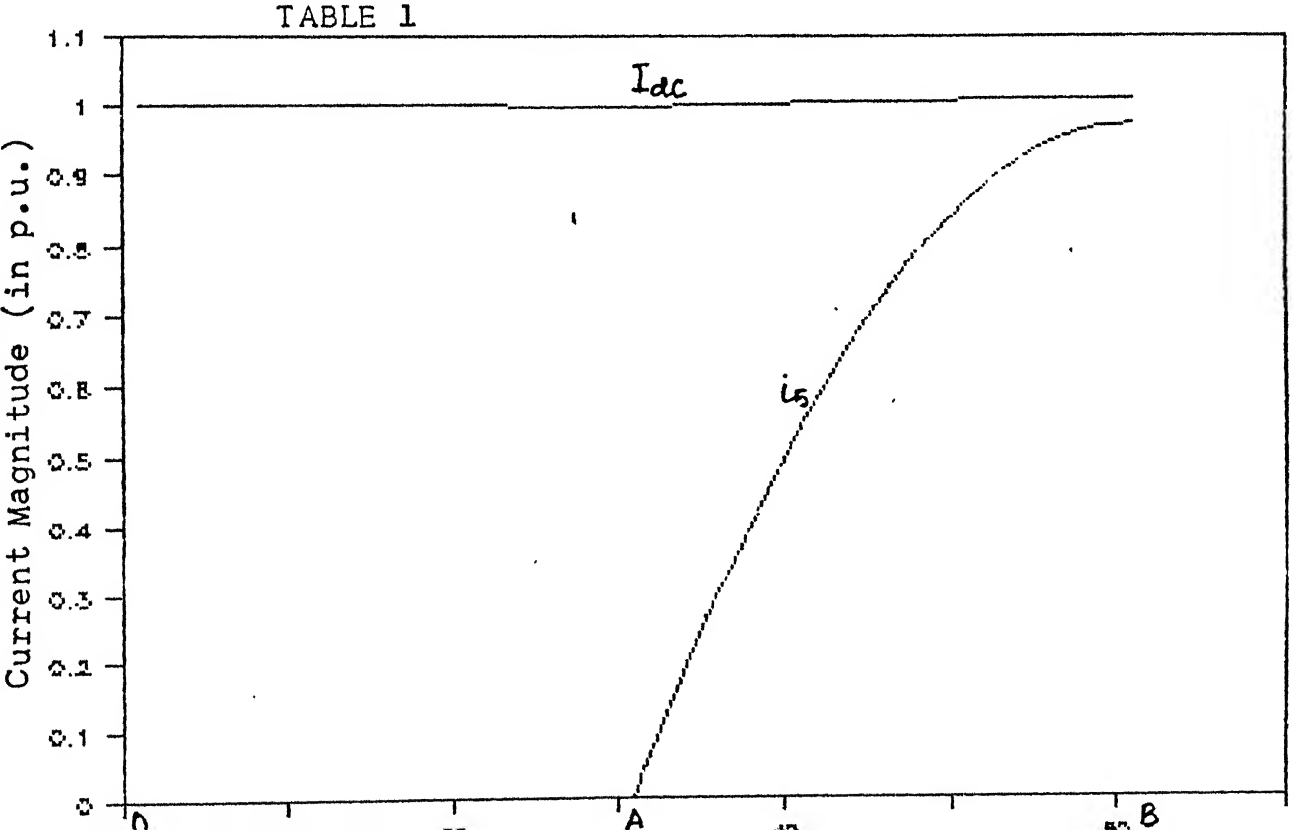



Fig. 2.9(c) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 3 OF TABLE 1



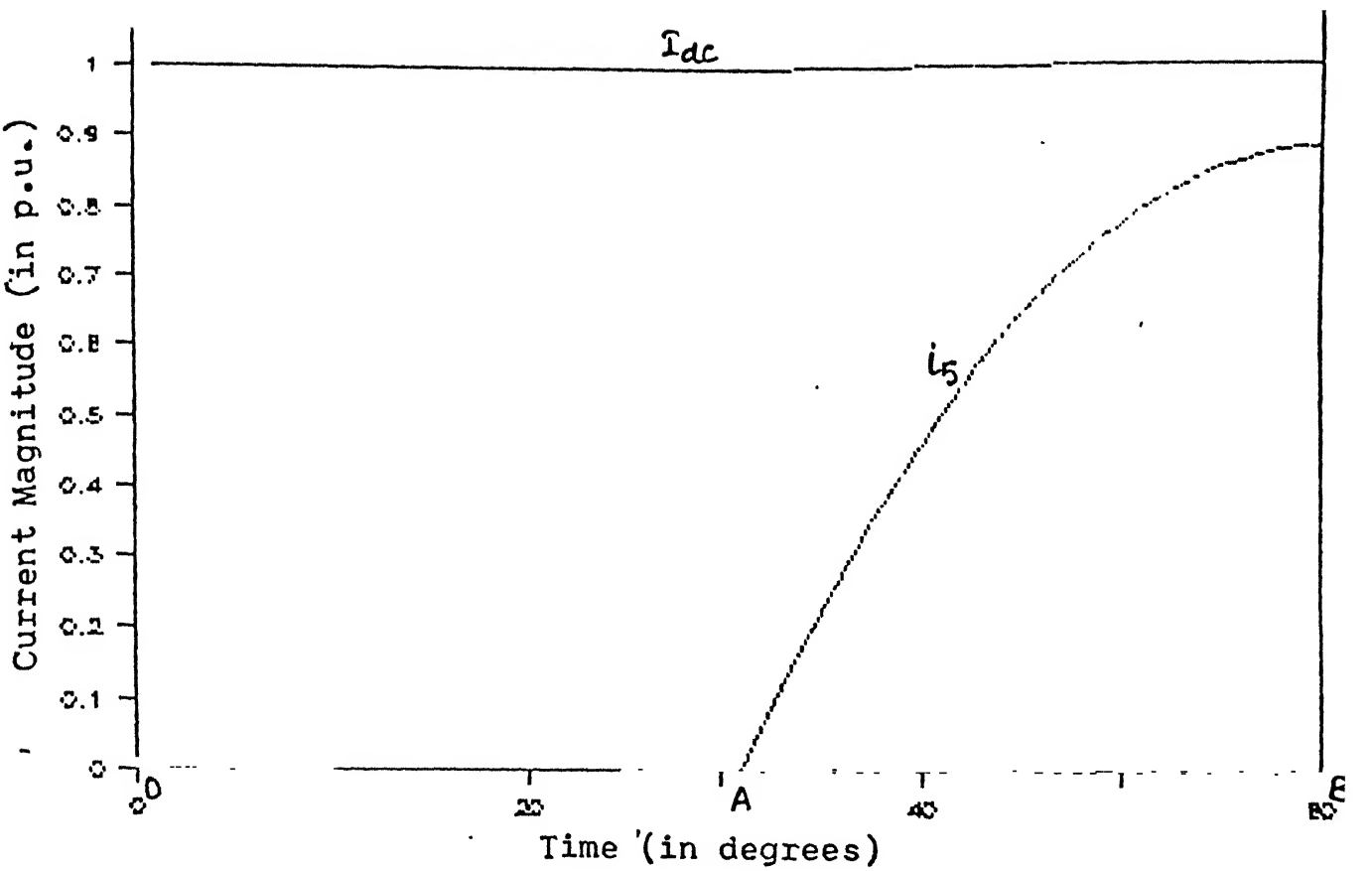



Fig. 2.9(e) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 5 OF TABLE 1

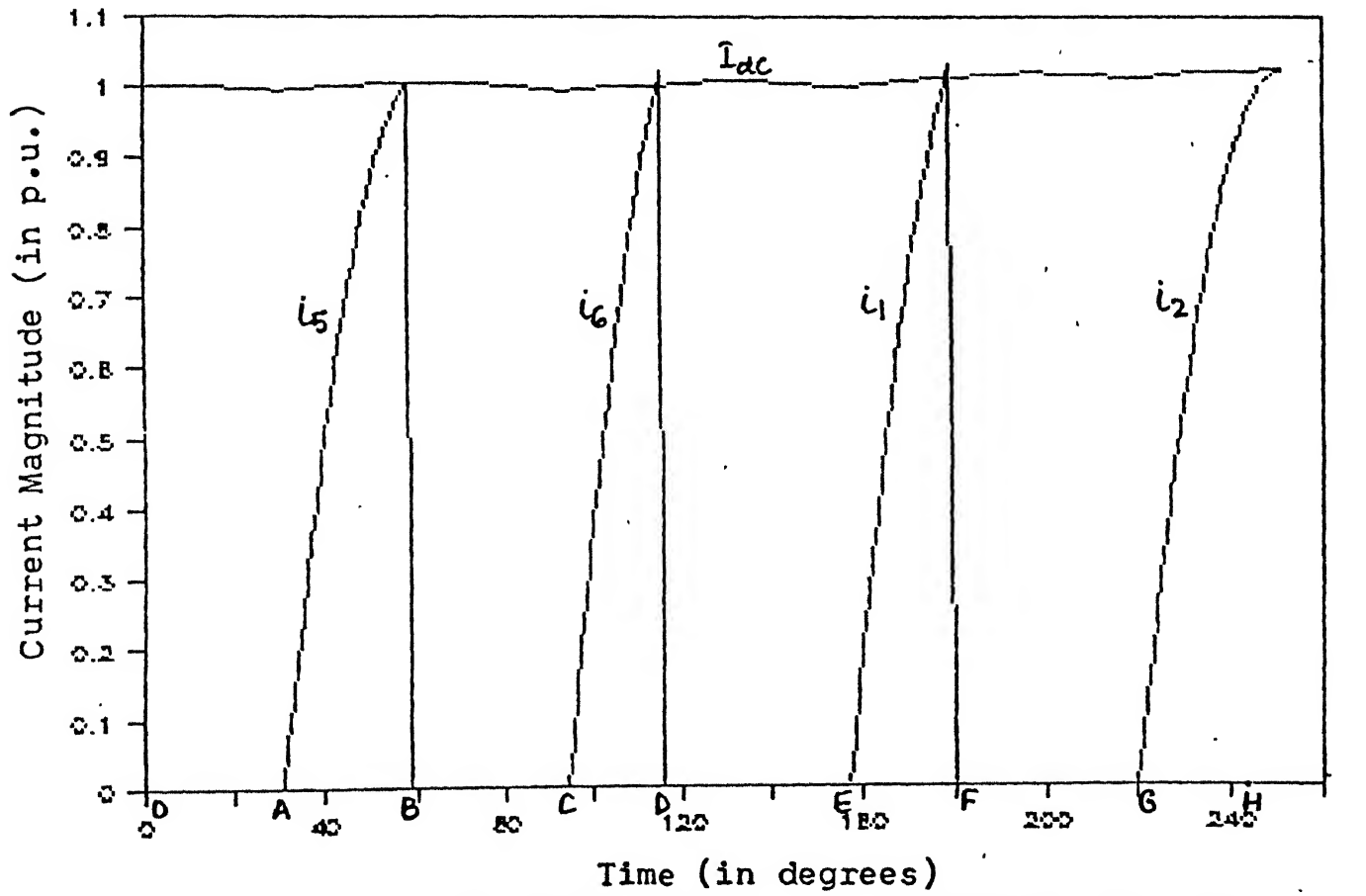



Fig.2.9(f) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 6 OF TABLE 1

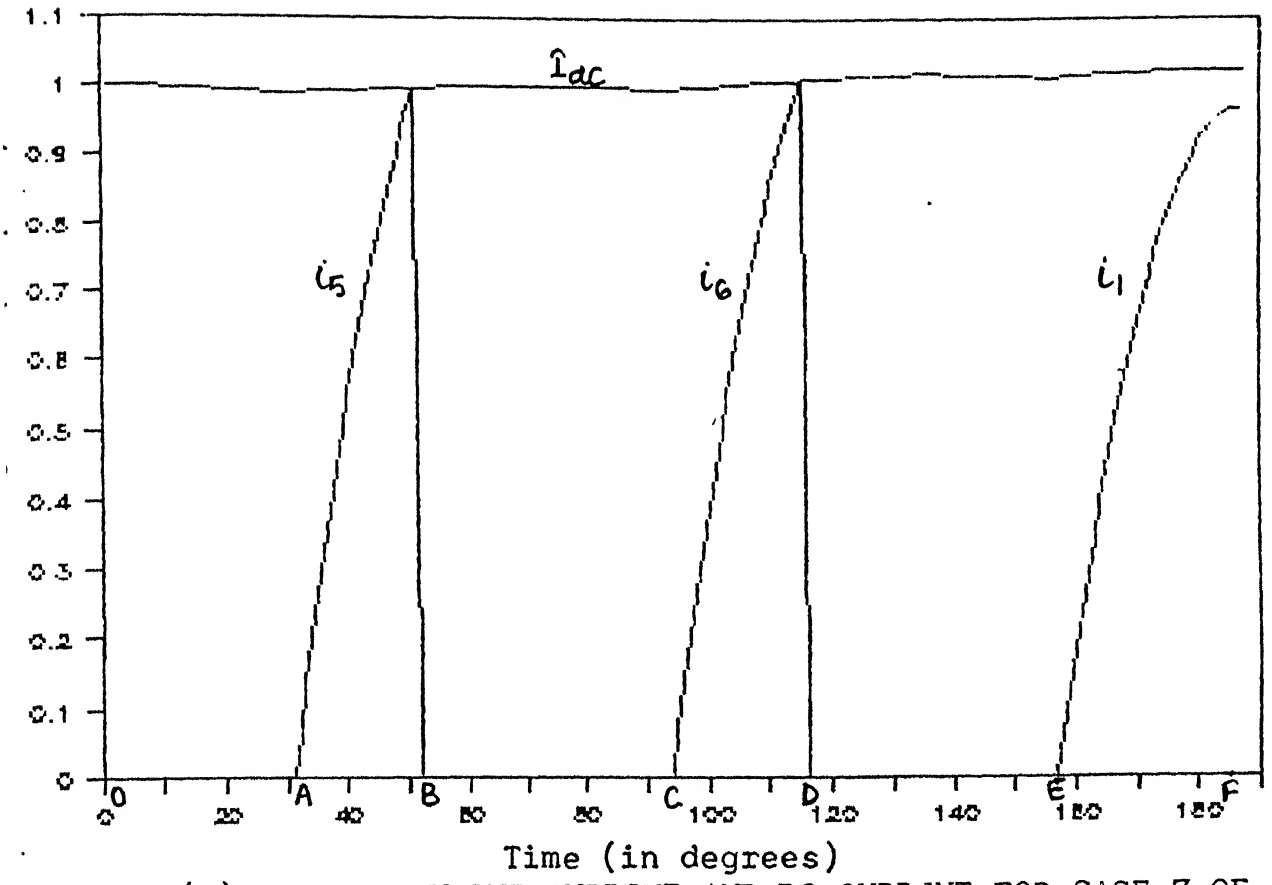
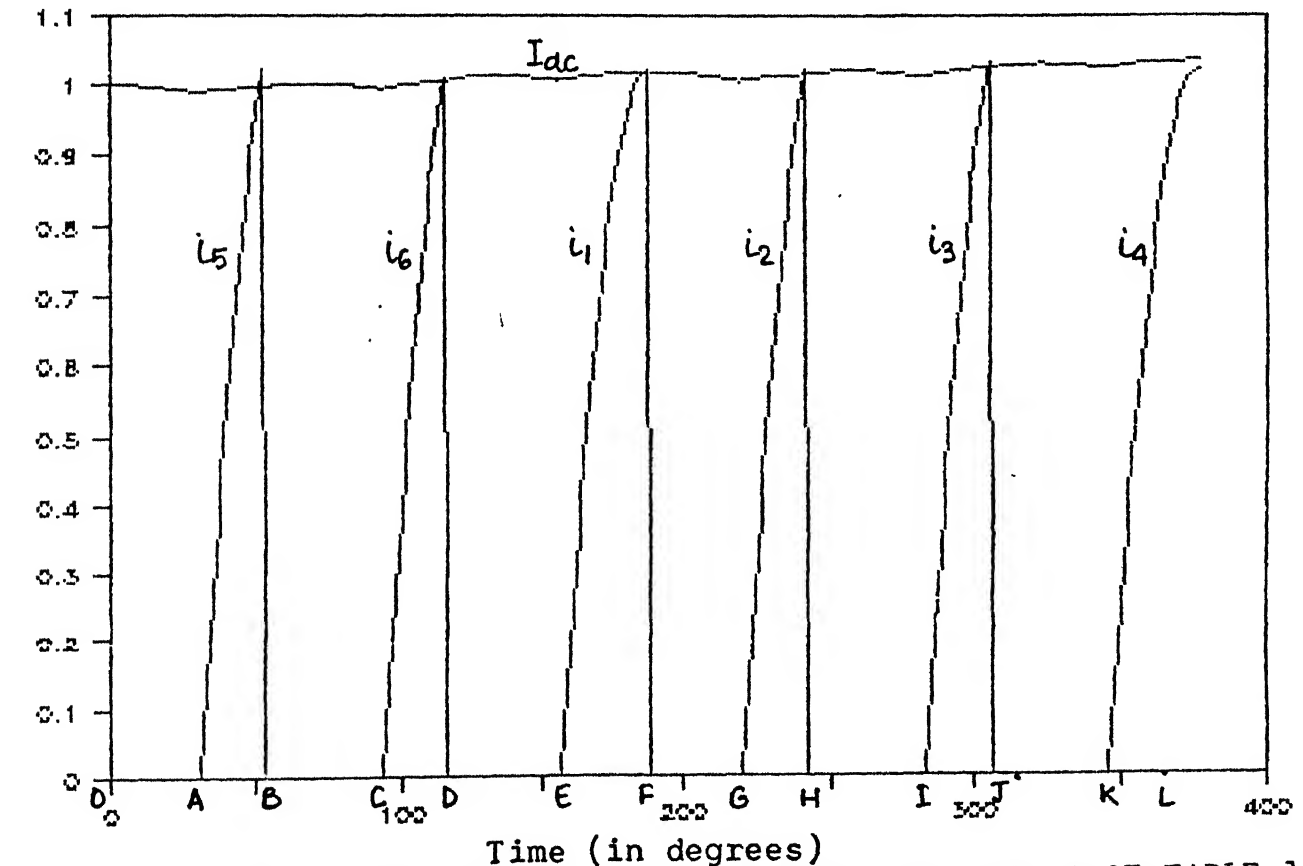



Fig. 2.9(g) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 7 OF TABLE 1




2.9(h) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 8 OF TABLE 1

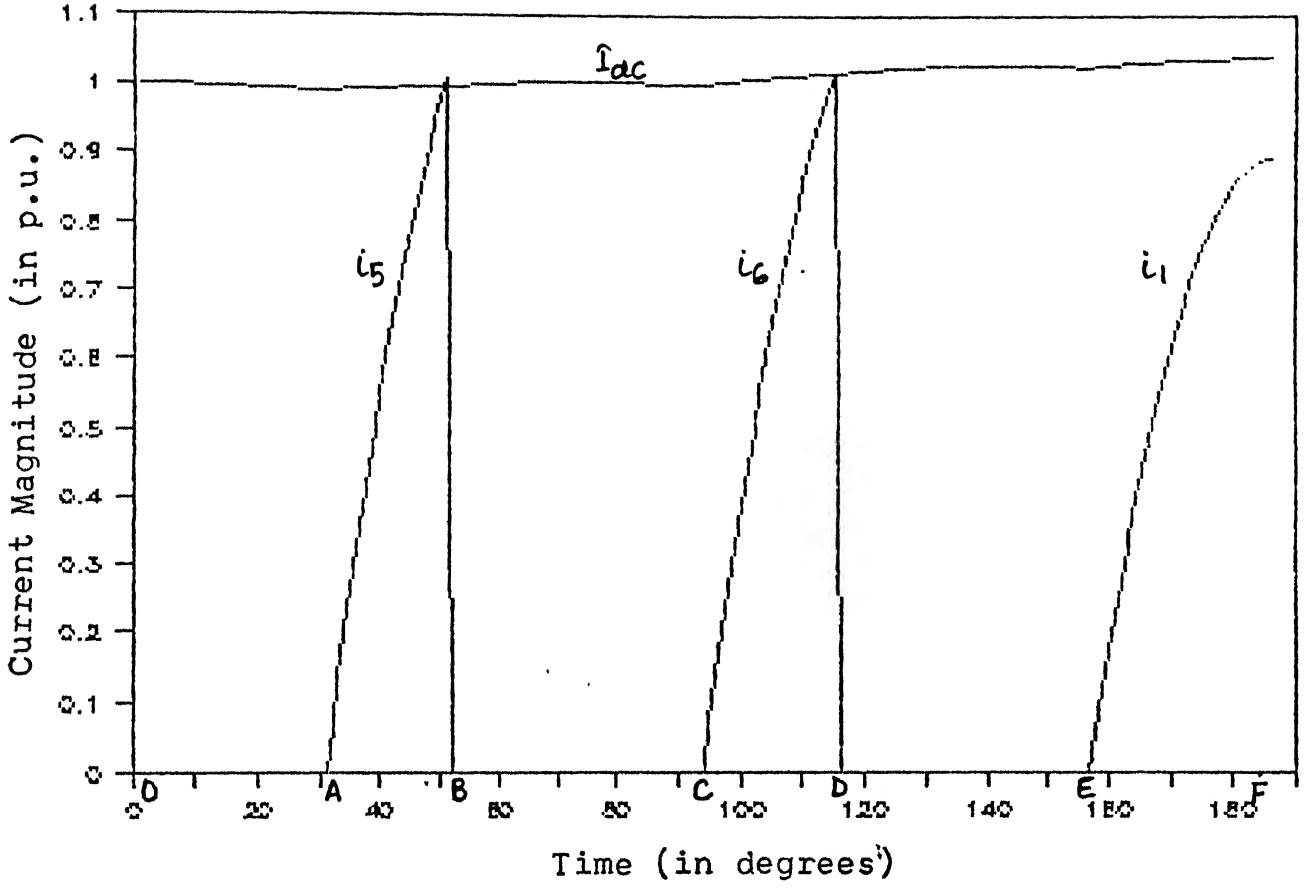



Fig. 2.9(i) INCOMING VALVE CURRENT AND DC CURRENT FOR CASE 9 OF TABLE 1

In Fig. 2.9(a) to Fig. 2.9(i) ;

$i_j$ where j = 1 to 6 is the current of incoming valve

$I_{dc}$ is the DC current

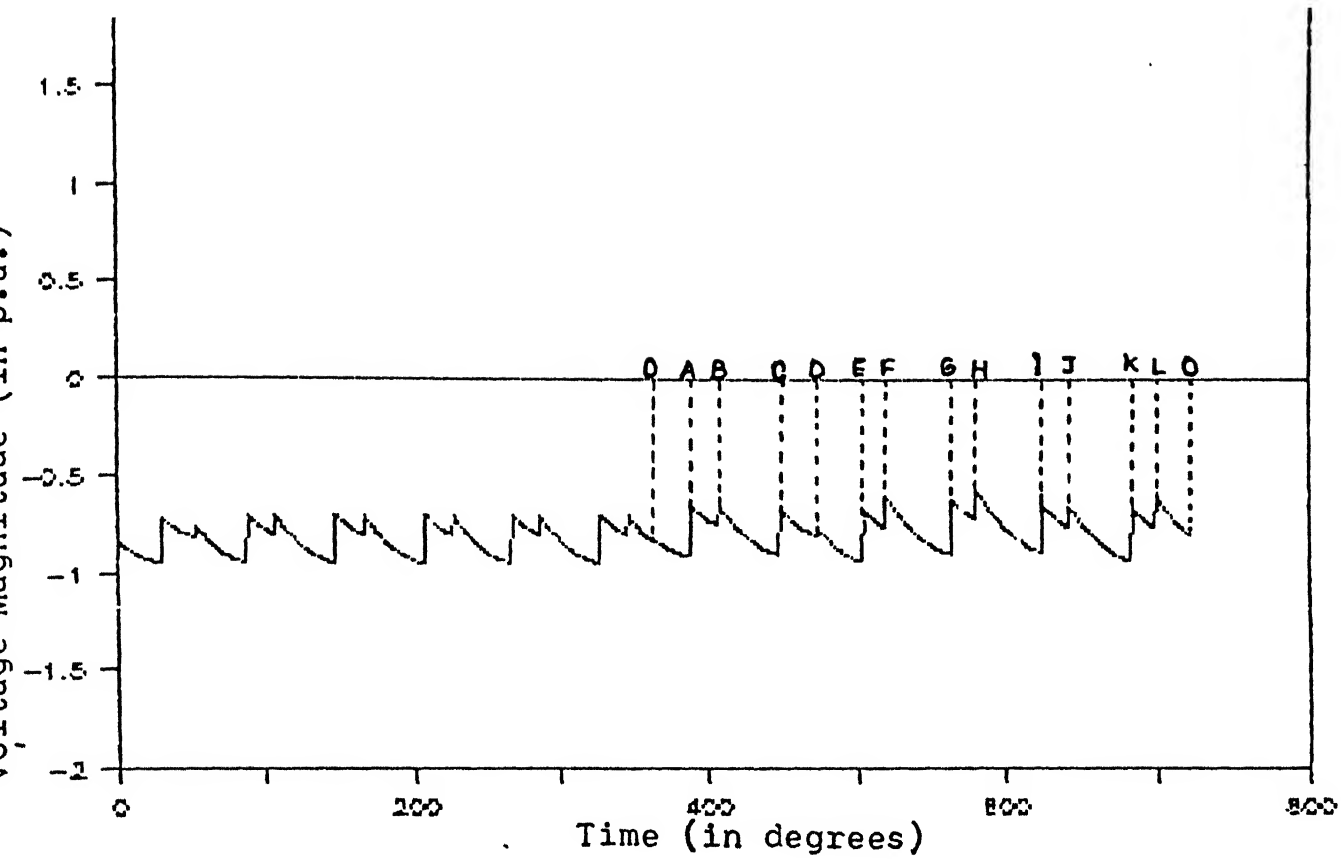
involving valves 4 and 6 and 1 and 3 respectively. It may be noted that both valves 1 and 4 are connected to phase A and are the outgoing valves in the respective commutation processes. A similar observation can be made in the cases where the dip occurs in phase B and C (cases 4 to 6 and 7 to 9 respectively). Therefore, from the various cases studied it can be concluded that commutation failure takes place only when the valves connected to the phase in which the dip has come become the outgoing valve in the commutation process.

It may be interesting to note from cases 3, 6 and 8 in table 1 that when the magnitude of dip in AC phase voltage is slightly higher than a critical value (a value below which no commutation failure occurs), the susceptible commutation process immediately following the instant of dip does not get affected. Instead the next commutation process which involves the valve in the dipped phase as the outgoing valve fails. This is because, the rise in the DC current which influences the commutation process is very gradual. This fact can be observed in Fig. 2.9(c) where following a 7% dip in phase A, the susceptible commutation process between valves 4 and 6 does not fail, but the commutation process between valves 1 and 3 fails.

In order to validate this conclusion, a detailed dynamic digital simulation of 2 terminal H.V.D.C. link was carried

out [3]. Digital simulation results are given in Fig. 2.10(a) to 2.10(d). These figures show the plot of DC voltage at the inverter terminal for a period of 2 cycles, with the dip considered in any one of the phase of the inverter end AC voltage. The dip is initiated at the beginning of the second cycle which is coincident with the instant $\omega t = 0$, corresponding to the positive going zero crossing of the commutation voltage of valve 1. Fig. 2.10(a) corresponds to a 10% dip in the inverter end phase A AC voltage. As can be observed this dip does not lead to any commutation failure at the inverter. This is because of the current control and constant extinction angle control actions at the rectifier and inverter terminals respectively. A similar case when studied based on the analysis given in Section 2.3 had indicated a commutation failure (case 2 of table 1). This indicates that the assumptions made in order to simplify the analysis of Section 2.3 lead to the worst case situation.

The results given in Figs.2.10(b) to 2.10(d) are obtained considering a 20% dip, initiated at the start of second cycle, in phases A, B and C respectively. The various valves conducting in the time regions OA , AB, BC etc. are the same as given in Table 1. It can be observed in Fig. 2.10(b) that valve 6 is fired at instant C and is not able to take up the link current in a stipulated margin. Hence, three valve conduction continues




. 2.10(a) INSTANTANEOUS INVERTER TERMINAL VOLTAGE FOR A 10% DIP IN PHASE A VOLTAGE

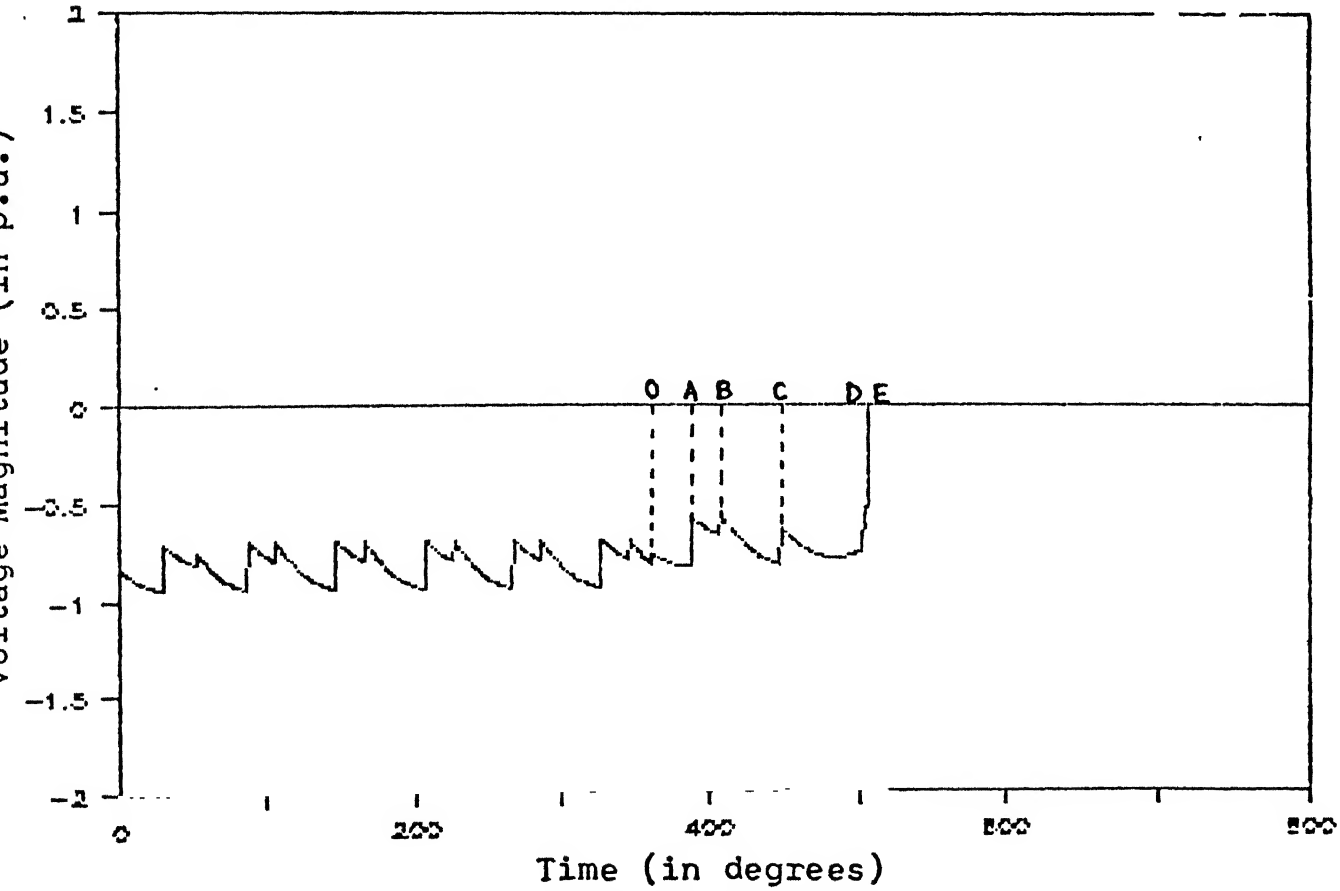
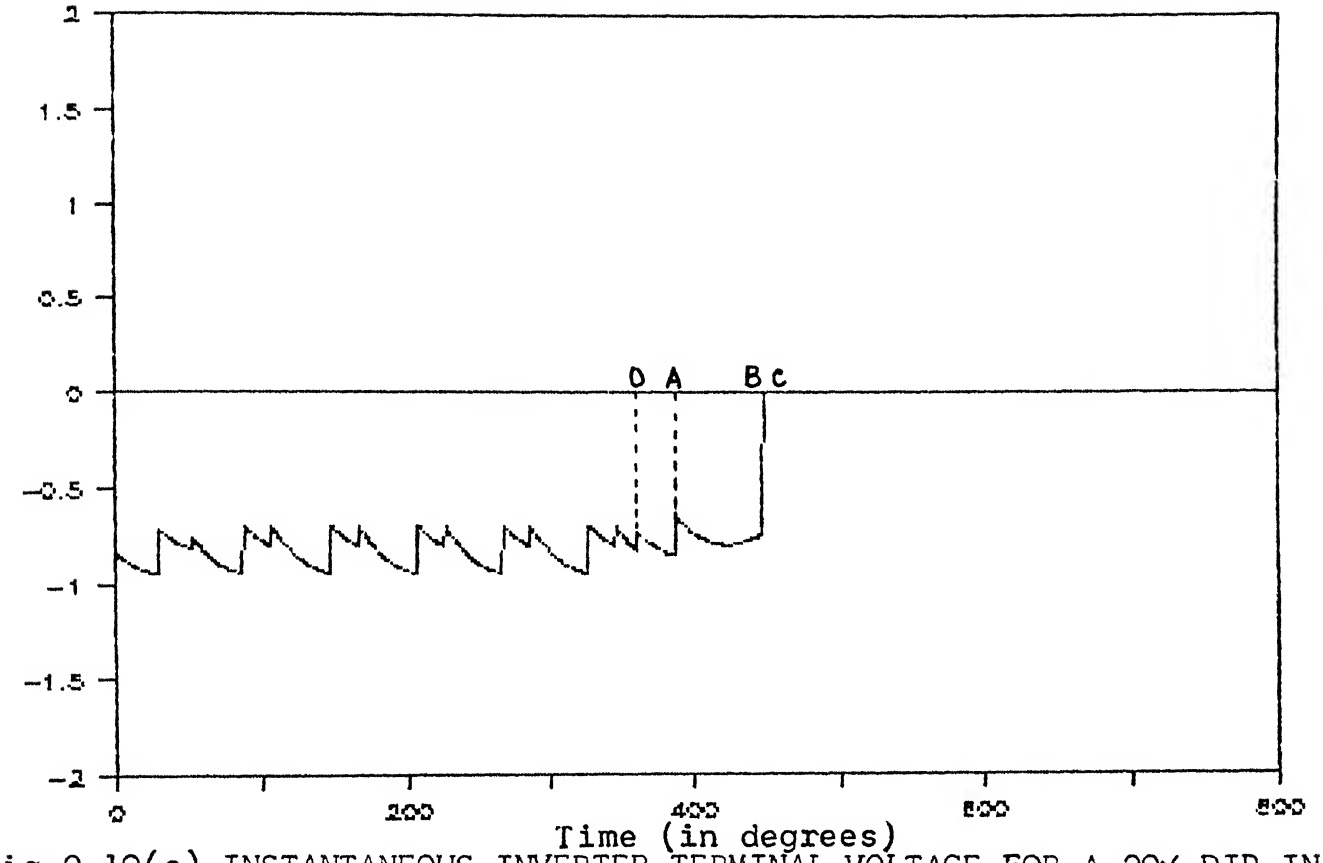
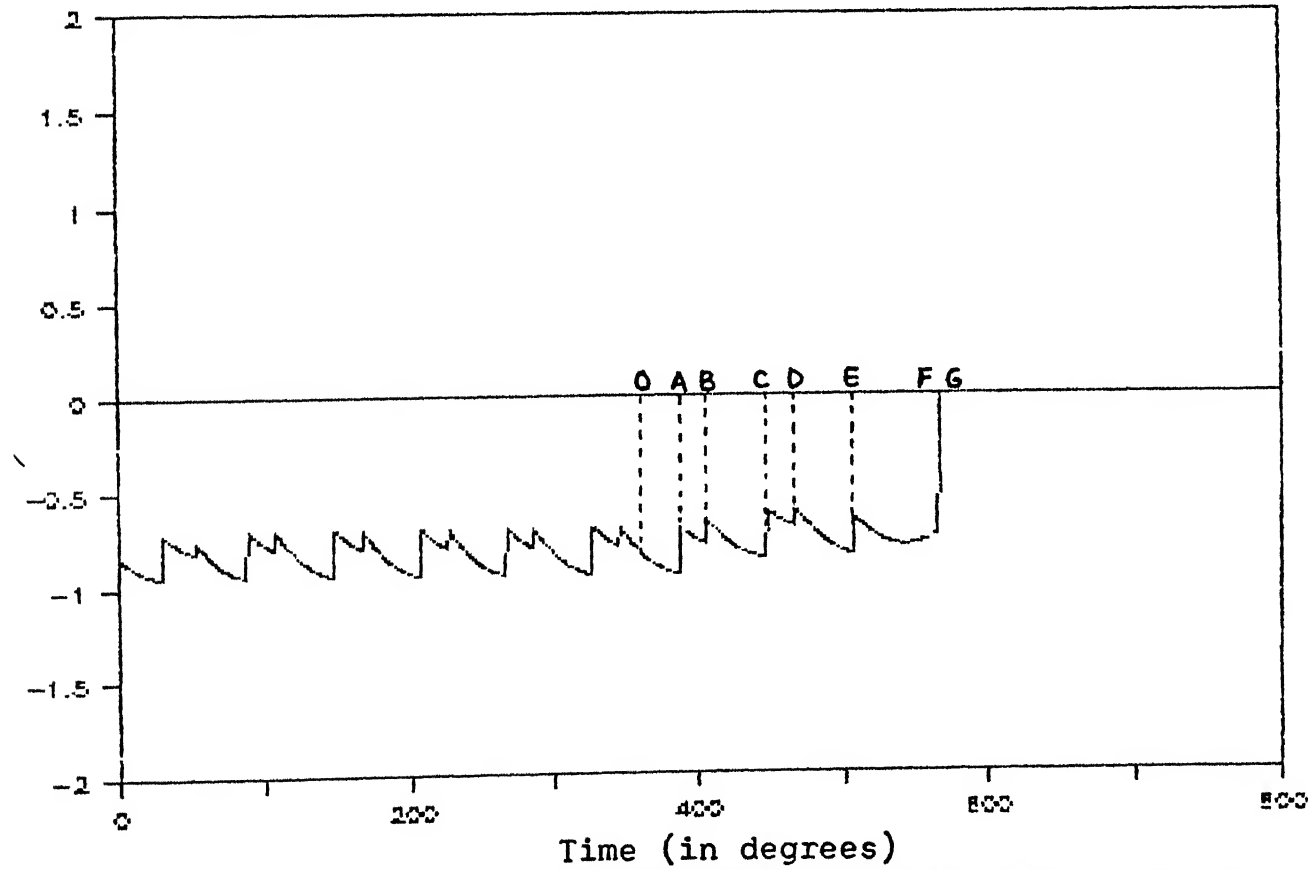



Fig.2.10(b) INSTANTANEOUS INVERTER TERMINAL VOLTAGE FOR A 20% DIP IN PHASE A VOLTAGE




ig.2.10(c) INSTANTANEOUS INVERTER TERMINAL VOLTAGE FOR A 20% DIP IN PHASE B VOLTAGE




ig.2.10(d) INSTANTANEOUS INVERTER TERMINAL VOLTAGE FOR A 20% DIP IN PHASE C VOLTAGE

till the next valve is fired at instant D thus resulting in a short circuit across the DC terminal due to 4 valve conduction. In this case also the commutation failure occurs during the commutation process of valves 4 and 6, which involves the dipped phase A as the phase of outgoing valve 4. Similar observations can be made in Fig. 2.10(c) and Fig. 2.10(d). Fig. 2.10(c) shows the inverter terminal voltage with a dip in phase B, and it can be observed that first commutation failure occurs during the commutation process of 3 and 5. This commutation process also involves phase B as the phase of outgoing valve 3. These observations validate the conclusion based on the results of simplified analysis drawn earlier.

### 2.5.2 Effect of the Instant at which Dip Occurs

To investigate the effect of the instant at which the dip occurs on the commutation process, various cases have been studied as listed in Table 2. It may be observed that for a dip of magnitude less than or equal to 6% there is no commutation failure irrespective of the instant at which the dip occurs. In case of 7% dip in phase A voltage the very first commutation process (either between the valves 4 and 6 or $1_{,3}$ ) which begins after the dip, does not get effected. Only the commutation process which begins later fails as described earlier with reference to Table 1 (case 3). However, for dips of larger magnitude, the first commutation process, which involves

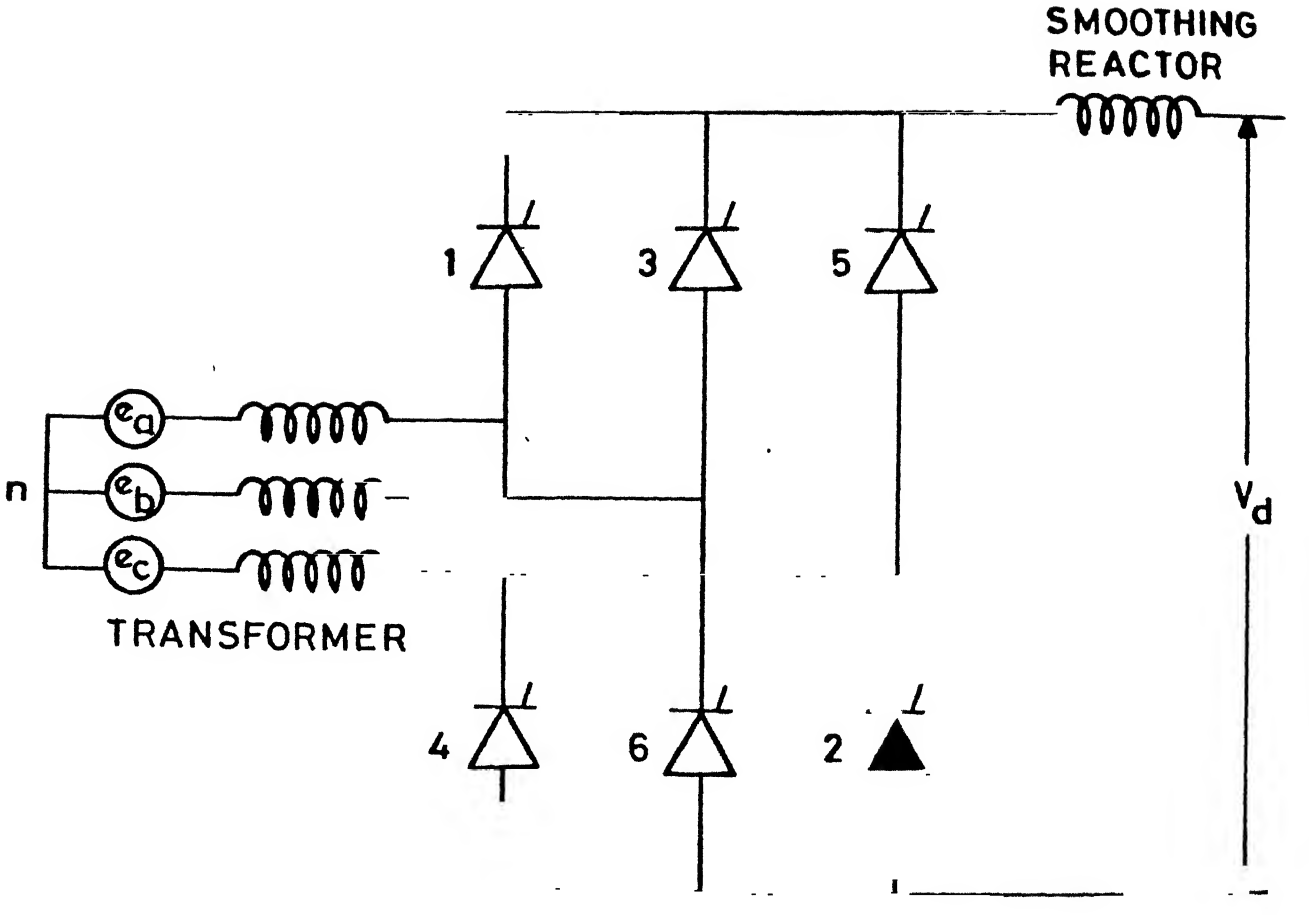



FIG. 2.1 (C) SIX PULSE BRIDGE CIRCUIT

Table 2
Effects of Instant at which dip Occurs on Commutation Process

| Phase of dip | Instant ωt | Magnitude of dip | Observations |
|---|---|---|---|
| A | any | 5% | No commutation failure |
| A | 148.38 | 6% | No commutation failure |
| A | 108.38 | 6% | No commutation failure |
| A | 98.38 | 6% | No commutation failure |
| A | 0 | 6% | No commutation failure |
| A | 81.38 | 7% | Commutation failure between valves 1 and 3 |
| A | 120 | 9% | Commutation failure between valves 4 and 6 |
| A | 148.38 | 7% | Commutation failure between valves 4 and 6 |
| A | 300 | 7% | Commutation failure between valves 1 and 3 |
| A | 50 | 8% | Commutation failure between valves 4 and 6 |
| A | 140 | 8% | Commutation failure between valves 1 and 3 |
| A | 108.38 | 8% | Commutation failure between valves 1 and 3 |
| A | any | 10% | Commutation failure during next commutation process involving phase A as the phase of the outgoing valve |

the valves in the affected phase as outgoing valves, itself fails.

Based on the observations of Table 2 it can be concluded that the instant at which dip occurs in the phase voltage does not influence the commutation process significantly.

## 2.6 CONCLUSIONS

In this chapter an analysis has been carried out to investigate the effect of the dip in the magnitude of the AC phase voltages and the instant of its occurrence on the commutation process of HVDC inverters.

It is observed that the commutation process is predominantly effected by the magnitude of the dip in the AC phase voltage. Also, the commutation failure takes place only when the valves connected to the phase in which the dip has occurred become the outgoing valves in the commutation process. This conclusion has been validated also through digital simulation study. A detailed information regarding the behaviour of the commutation process is helpful in designing an effective converter control system.

# CHAPTER 3

## RECOVERY SCHEMES FOR COMMUTATION FAILURE

### 3.1 INTRODUCTION

Any disturbance in the AC phase voltage on either the rectifier or the inverter end of HVDC link influences the performance of the HVDC system. The impact of the disturbance (line to ground or 3-phase to ground fault at the converter AC bus or at any remote bus in the AC network) i quite severe particularly when it is in the AC phase voltage at the bus, where inverter is connected. Such voltage distu: bances, which may vary in magnitude, invariably lead to comm tation failure at the inverter terminal. To minimise the effect of commutation failure and help the system recover fas the converter control system is suitably designed. Thus one of the major objectives of the converter control is to help the system recover to its normal operation at the earliest. This is achieved by suitably varying the firing instants of various valves after the occurrence of the disturbance. The variation in the firing instants is governed by the dynamics of the converter controller and firing pulse generating syste In this chapter the converter recovery procedure following a commutation failure is studied in detail. Also a need for

having an additional control to enhance the recovery proce: is explored and certain suggestions are made in this conte:

## 3.2 COMMUTATION FAILURE AND RECOVERY PROCESS

Considering that a two terminal HVDC link is under nor operation before a substantial dip in phase A ac voltage oc at the inverter end at the instant $\omega t = 0$, which is coincid with positive going zero-crossing of the commutation voltag valve 1. As a result of this voltage disturbance the commu tion process between valves 4 and 6 fails [refer Fig . 2.9(l and valve 4 continues to conduct beyond its scheduled condu· ction period. The other valve conducting in the bridge is \ 5. The next valve to conduct is valve 1 and comes into conc ction $60^{\circ}$ later than the instant at which the valve 6 came i conduction. The time interval between the conduction instan of valves 1 and 6 will be $60^{\circ}$ because the inverter is operat under constant extinction angle control. As soon as valve 1 c into conduction a short circuit is established across the in ter DC terminals due to the conduction of valves 1 and 4. F ther, the commutation process between valves 5 and 1 will be successful as valve 1, which is connected to the dipped phas is not the outgoing valve. The next valve to come into condu ction is valve 2. The firing pulse for this valve, although would be released by the inverter control system, the valve cannot come into conduction as the voltage across it would be

of Figs. 3.1(a) and 3.1(b) which show the ac phase and commu tation voltages following a dip in phase A. The voltage acr valve 2 in the event of commutation failure between valves 4 and 6 will be $e_{ac}$. The instant at which the firing pulse fo valve 2 is released lies in the interval CE [Fig. 3.1(b)]. This instant again is $60^{o}$ later (due to CEA control) than th instant at which the firing pulse for valve 1 was released. Beyond instant C it can be seen that voltage $e_{ac}$ is negative a period greater than $120^{o}$ which is normally the duration of firing pulse. Thus valve 2, cannot come into conduction anc the short circuit continues across the DC terminal. With the firing of the next valve the commutation process between valves 1 and 3 fails as the valve 1 connected to dipped phase is outgoing valve. Since valve 4 is still conducting the nex valve which can start conduction is valve 5 but it fails to begin conduction for the reason similar to that of valve 2. long as the dip in phase A persists, valve 1 and 4 keep condu cting resulting in short circuit across DC terminal. In cas the dip is removed before valve 6 comes into conduction the commutation process between valves 4 and 6 will be successful provided the rectifier current controller has been able to restrict the link current to its rated value. If so, the converter recovers to its normal operation.

From the above discussion it is evident that for a fast recovery it is essential that the short circuit across the

inverter terminals must be removed at the earliest. One way to accomplish this is to advance the firing of the subsequent valves which would come into conduction after the occurrence first commutation failure. This approach, examined in detail in the next section, might help avoid further commutation failures.

## 3.3 SCHEME TO IMPROVE RECOVERY PROCESS

Commutation failures mainly occur because of the lack of sufficient time margin for the incoming valve to take up the link current from the outgoing valve. This reduction in the margin is mainly because of dip in the a.c. phase voltage and shift in the zero-crossing of commutation voltages resulting in reduced voltage time area required for successful commutation [4]. This indicates that the chances of successful commutation can be improved by increasing the margin available for the commutation process which can be done by advancing the firing of the valves. This has been the philosophy behind all the recovery schemes proposed so far [5]. The only difference in various schemes lies in the manner in which the firing is advanced. The recovery scheme described in this chapter is also based on the same philosophy.

The theory involved in the recovery scheme can be explained with the help of Fig. 3.1(b), which shows the commutation voltage waveforms for a dip of 50% in phase A. For the inverter firing

angle ($\alpha$) of $150^{\circ}$, there will be valves 3, 4 conducting at $\omega t = 0$. Valve 5 will be fired at $\omega t = 30^{\circ}$. Since the commutation process 3, 5 does not involve phase A, there will be no commutation failure. Valve 6 will be fired at the instant $\omega t = 90^{\circ}$. Since the commutation process 4, 6 involves phase A as the phase of the outgoing valve hence, there will be a commutation failure. In the commutation process initially the current through the incoming valve increases and that through the outgoing valve 4 decreases till instant B beyond which the valve 6 current starts decreasing and that of valve 4 starts increasing, thus resulting in commutation failure. Instant B is coincident with the negative going zero-crossing of the commutation voltage of valve 6. In the proposed recovery scheme next valve (valve 1) is fired immediately at the instant B. As a result 4 valves (4, 5, 6, 1 will be conducting beyond instant B thus creating a temporary 3 phase short circuit at the inverter. In a short time valves 1 and 4 will completely take over the link current and valves 5 and 6 will cease to conduct. At this instant the next valve 2 is fired. It can be seen from Fig. 3.1(b) that valve 2 is fired in the region BD. The exact instant of its firing depends on the time elapsed from instant B till only two valves (1 and 4) are conducting. In the absence of this forced firing it can be seen that valve 2 will not come into conduction because in the region CE the voltage across valve 2 is negative. With

the conduction of valve forced in the region BD the inverter operates under 3 valve conduction mode with valves 1, 2, 4 conducting. Since there is a sufficient time margin availabl before the voltage $e_{ac}$ across valve 2 zreverses at instant C, the commutation process between valves 2 and 4 will be succes: ful. This leads to the removal of the short circuit across tl inverter DC terminal which otherwise would have continued unless the AC phase voltage recovers to its normal value. It may be mentioned that the forced firing of valve 2 results in a firing angle less than $90^{o}$ i.e., rectifier region. Once rvalve 2 is fired the next valve 3 is fired at an instant such that the firing angle is greater than $90^{o}$ and preferably aroun $120^{o}$. The subsequent valves are fired at appropriate instants determined from current or extinction angle controller. The additional firing requirements described above not only lead to fast recovery following a commutation failure, but also reduces the duration of temporary voltage collapse across inverter DC terminal.

## 3.4 CASE STUDY

The effect of additional firing requirement described in the previous section is investigated in detail through digital simulation of two terminal HVDC system. The operating conditions and parameters are given in Appendix A. The effectiveness of the proposed recovery scheme is examined in the events of

i) A short duration single phase to ground fault either at a remote location in the AC system or at the invert AC bus.

ii) A prolonged single phase to ground fault either at any remote location in the AC system or at the inverter AC bus.

iii) A three phase to ground fault either at any remote location in AC system or at the invèrter AC bus.

In the digital simulation program these faults are simula ted by appropriately modifying the magnitudes of the AC voltag source connected to the inverter terminal. This modification is initiated at an instant of time corresponding to the occurrence of the fault and persists for the duration of fault. The rectifier and the inverter terminal are considered to be equipped with both the constant current and constant extinction angle controller. The firing pulses are generated using digital techniques [6]. The detailed representation of the HVDC system for the purpose of digital simulation is described in [7].

### 3.4.1 A Short Duration Single Phase to Ground Fault

In this section the following faults are considered :

a) 20% dip in phase A voltage

b) 50% dip in phase A voltage

c) single phase to ground fault.

The response of the system following the fault in case (a) are given in Figs. 3.2 and 3.3. Fig. 3.2 shows the response of the system following a single cycle 20% dip in phase voltage at inverter terminal without considering the additiona firing requirements. This recovery is achieved with the help of current control and extinction angle control at the rectifier and inverter terminals. This recovery process henceforth is termed as the normal recovery process. The effect of advancing the firing angle (as described in Section 3.3) on th system response is demonstrated in Fig. 3.3. From the compara tive study of the plots shown in Fig. 3.2 and Fig. 3.3 followi points can be noticed :

i) The short circuit at the invertor terminal persists for almost 4 cycles in case of normal recovery process, where in case of the proposed recovery scheme, the short circuit is almost avoided, hence improving the system recovery. The exact manner in which the firing is advanced can be explained with the help of Fig. 3.4. Fig. 3.4(a) shows the instantaneous inverter terminal voltage and Fig. 3.4(b) shows the inverter firing angle over a period of two cycles. From Fig. 3.4(a) it is evident that there is a commutation failure between valves 4 and 6. The scheduled instant at which valve 1 was supposed to come into conduction is instant C. But in the proposed recovery scheme

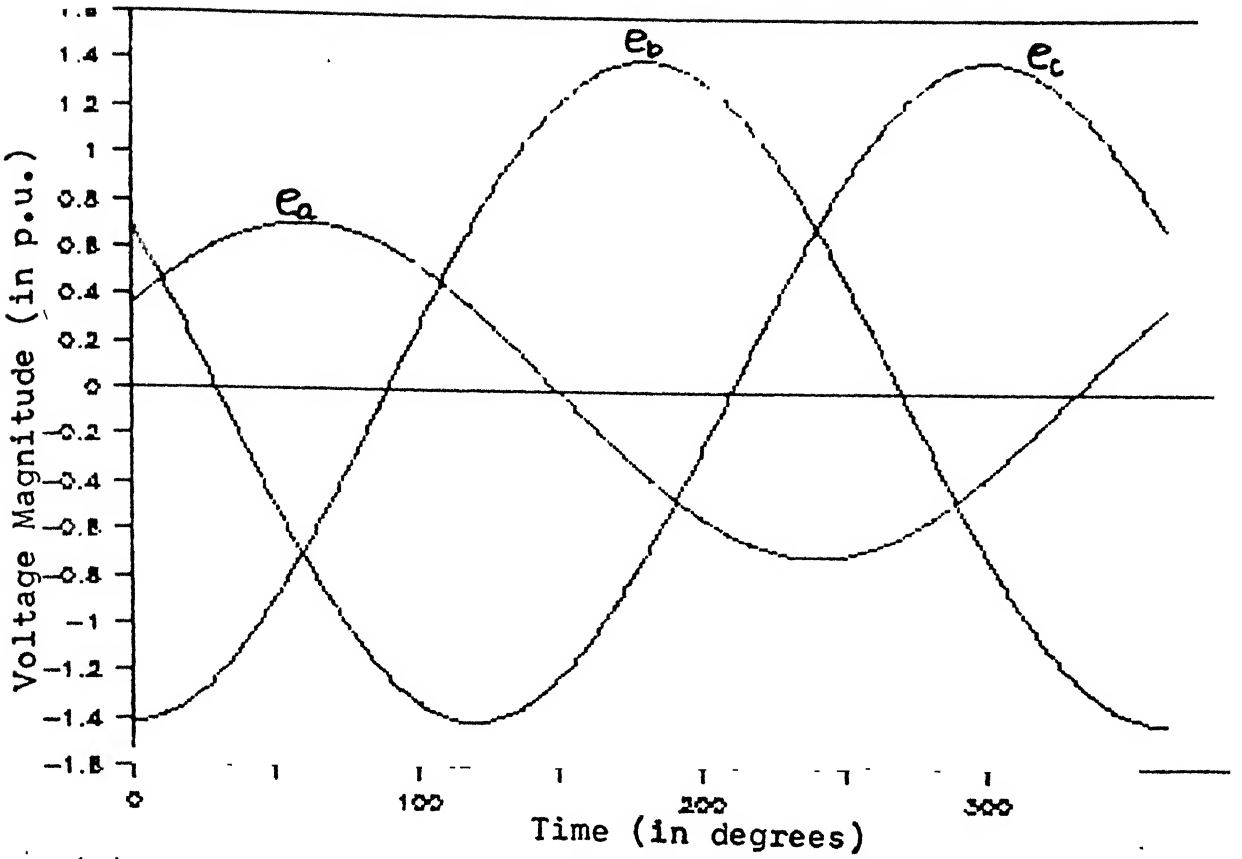
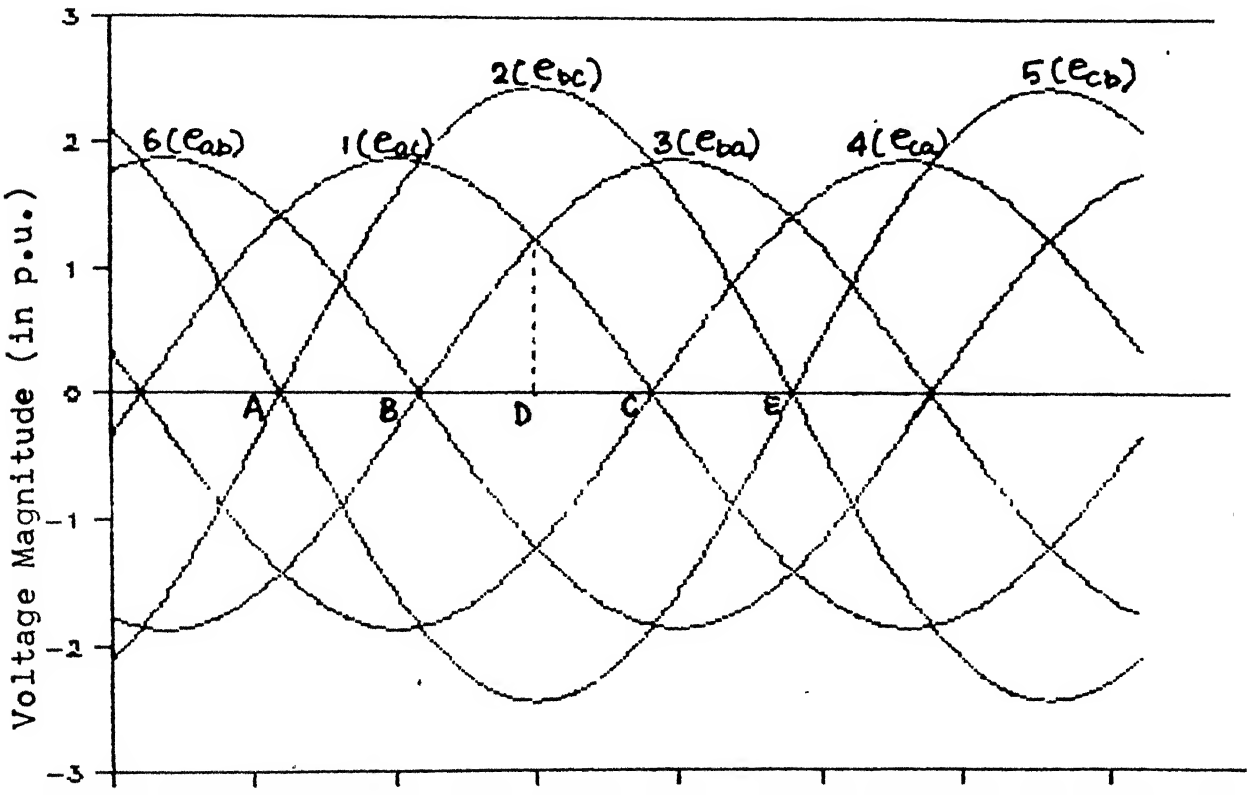
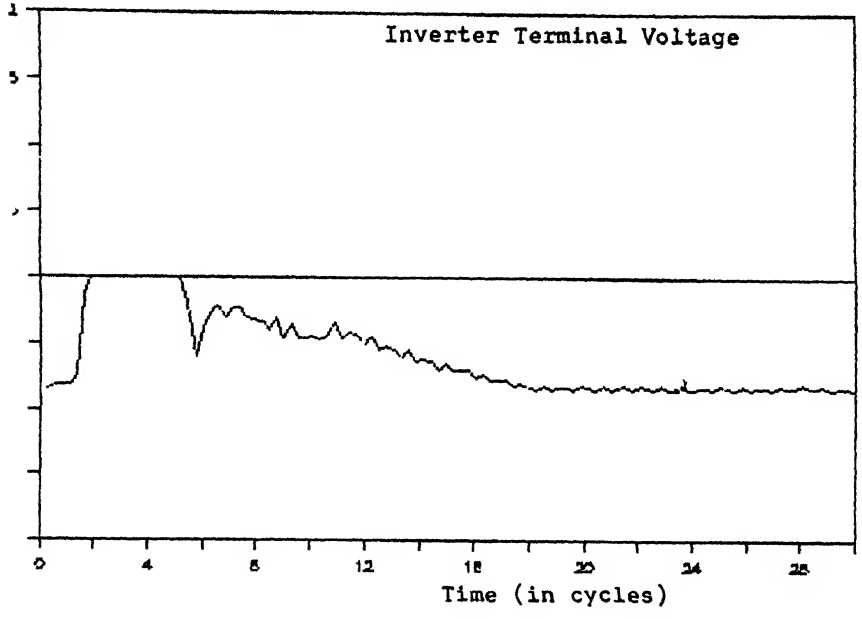
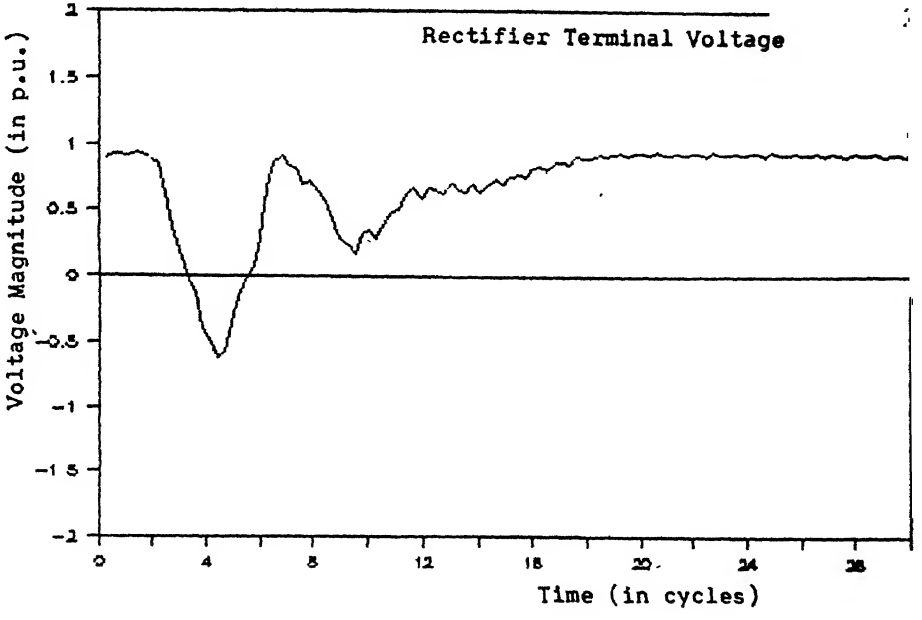
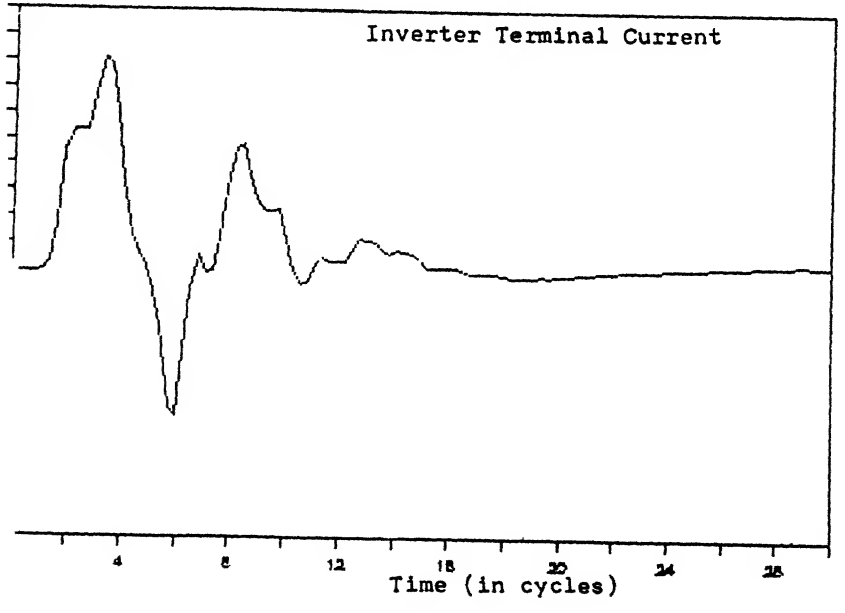


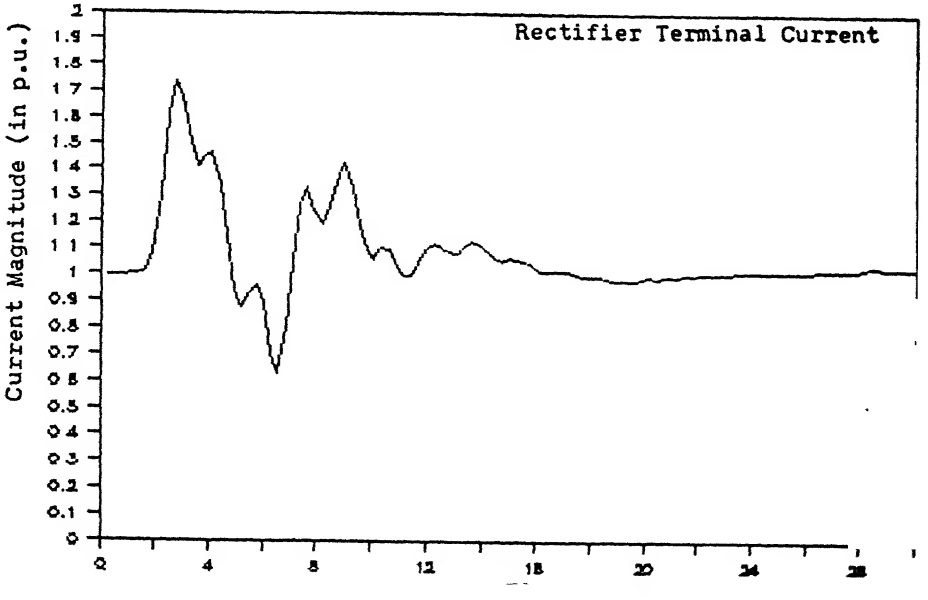

Fig.3.1(a) AC PHASE VOLTAGES FOLLOWING A DIP IN PHASE A

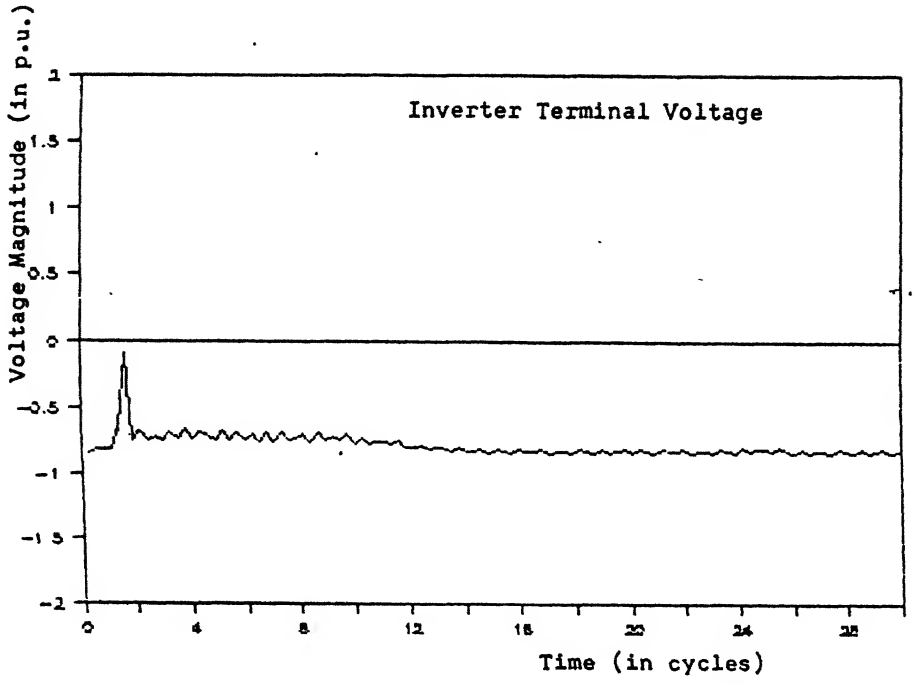


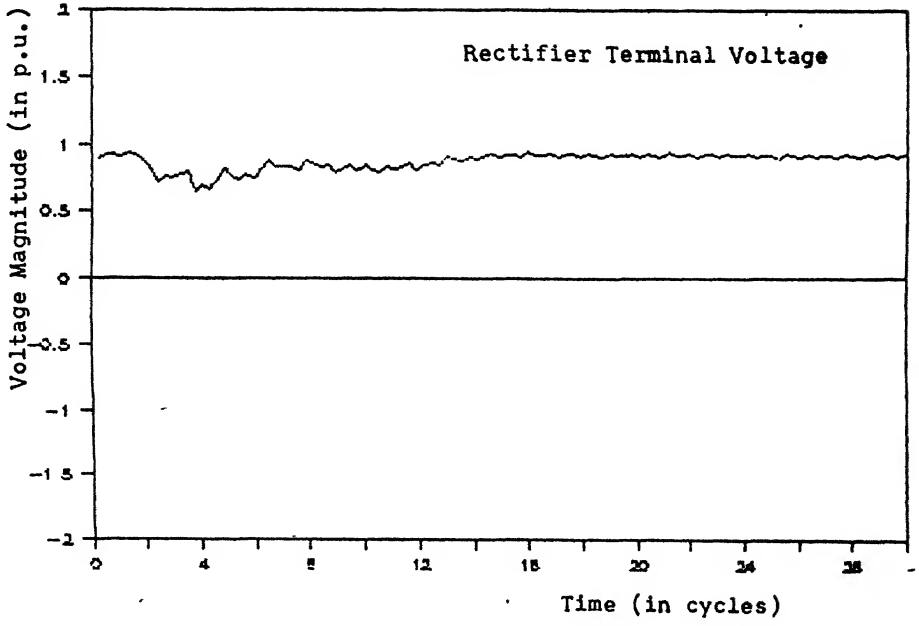

Inverter Terminal Voltage
Time (in cycles)

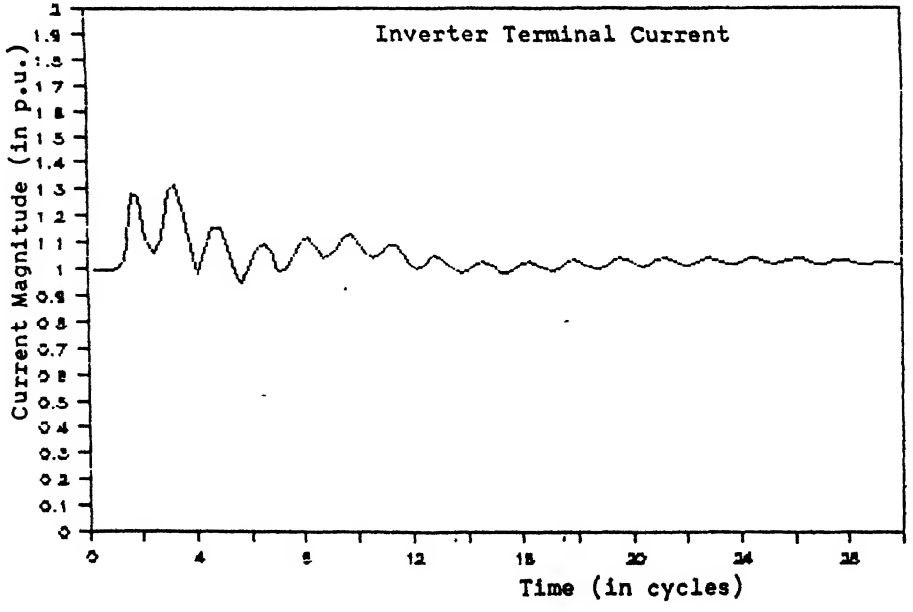

Rectifier Terminal Voltage
Voltage Magnitude (in p.u.)
Time (in cycles)


Inverter Terminal Current
Time (in cycles)


Rectifier Terminal Current
Current Magnitude (in p.u.)



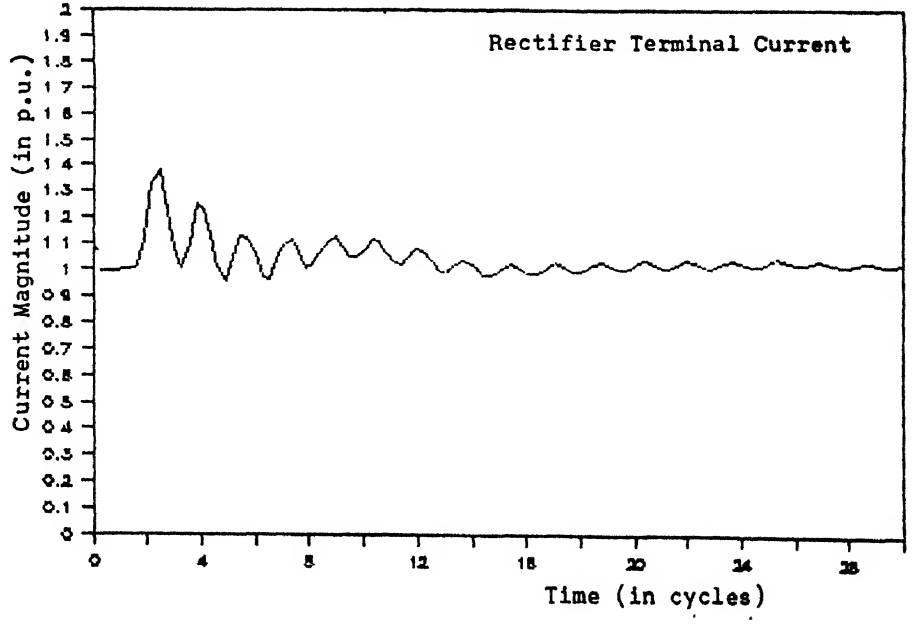
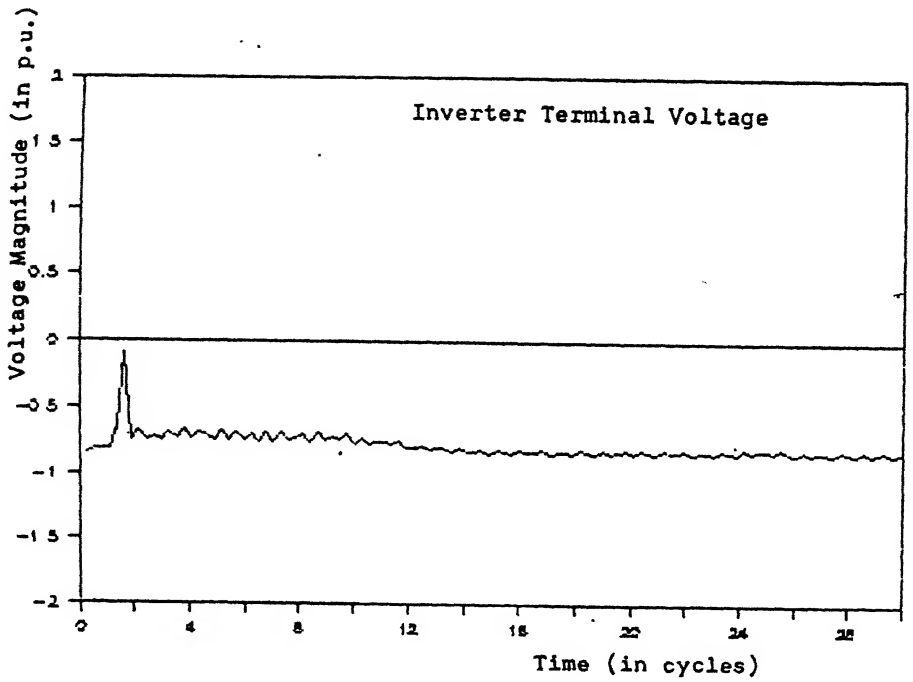
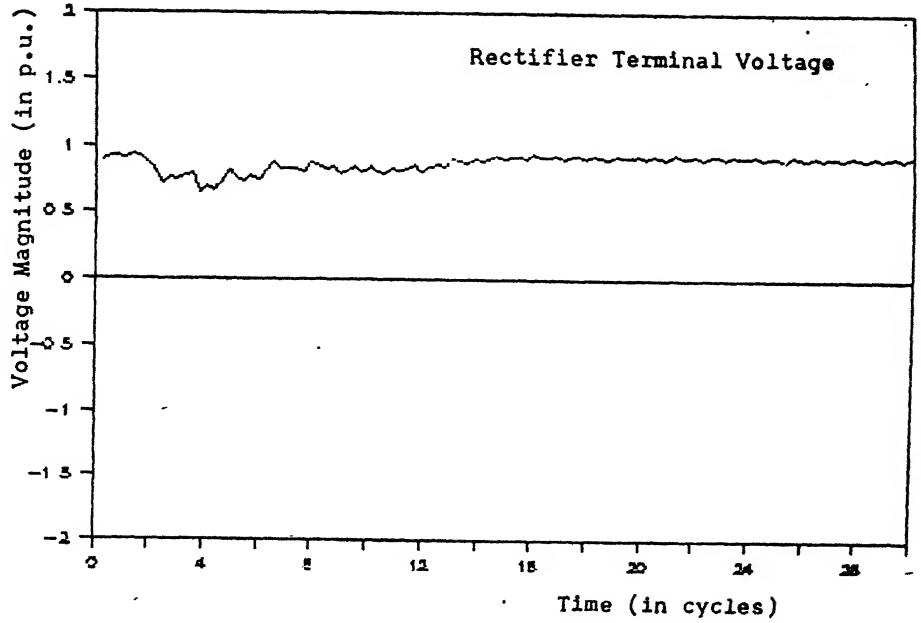
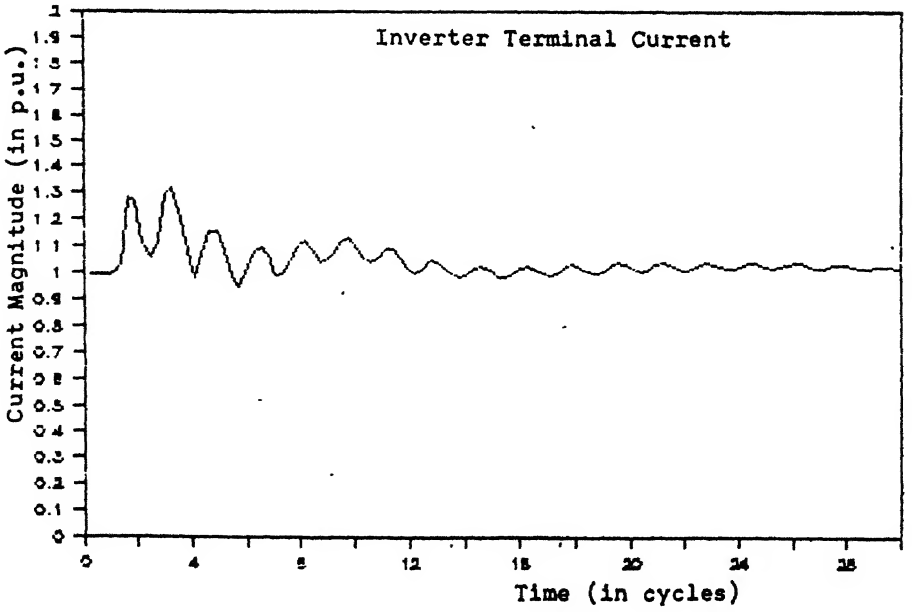




Fig. 3.3 20% SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



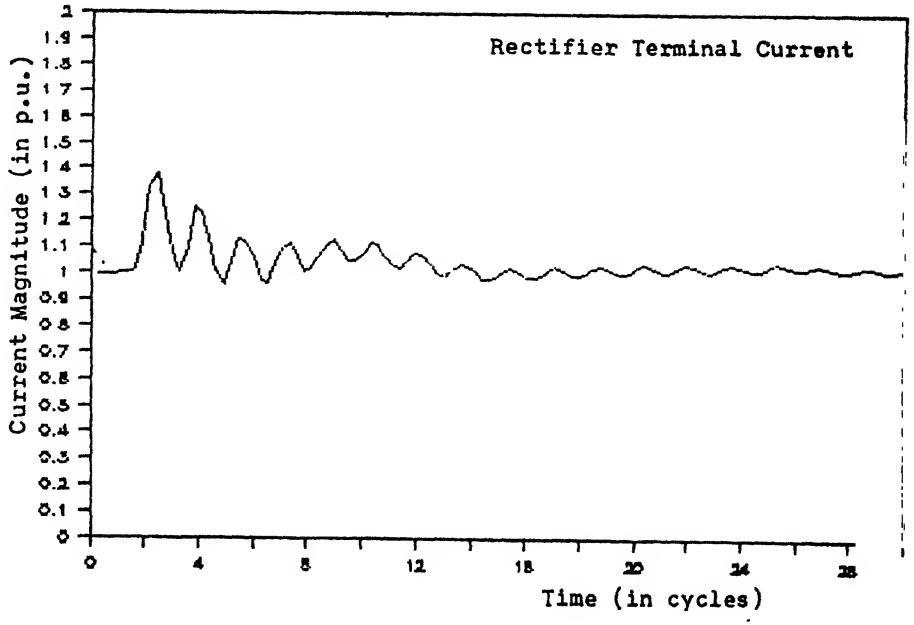




Fig. 3.3 20% SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME

the valve is fired at the instant C', thus deliberately creating a short circuit at the inverter terminal. At instant C' the value of the firing angle for valve 1 is $110^{\circ}$ (refer Fig. 3.4(b)). This forced firing of valve 1 will result in turning off of the valves 5 and 6 as valves 1 and 4 will completely take over the current. As soon as valves 5 and 6 turn off valve 2 is fired, which in Fig. 3.4(a) is instant D'. At instant D' the value of the firing angle of valve 2 is $77^{\circ}$ (refer Fig. 3.4(b)), hence firing it in rectifier zone. As a result the instantaneous terminal voltage will be positive for a short duration of time. However, the average DC voltage at the inverter terminal will be negative (refer Fig. 3.3). This advance in the firing of valves 1 and 2 avoids subsequent commutation failure and helps system recover fast.

ii) The current waveform with the proposed recovery scheme has oscillations with low peak value. It can be noticed that peak value of link current in case of normal recovery process is around 1.8 p.u. (refer Fig. 3.2) whereas with the proposed recovery scheme the peak is only of the order of 1.3 p.u. but it has more subsequent oscillations as compared to the normal recovery process.

iii) Rectifier terminal voltage has large oscillations in case of the normal recovery process because of the longer duration of the short circuit at the inverter DC terminal (refer Fig. 3.2) whereas with the proposed recovery scheme

those oscillations are reduced to a great extent because of the reduction in the duration of temporary voltage collapse across inverter terminals.

Based on the above noticed facts it is obvious that the proposed recovery scheme is quite effective for short duration remote faults. In the proposed recovery scheme discussed so far, a deliberate short circuit across terminal is created immediately on the detection of an imminent commutation failure. However, an alternate possibility has also been explored where the next valve is fired after actual commutation failure takes place. The results for the fault in case A with this modification has been reported in Fig. 3.5 and Fig. 3.6. Fig. 3.5 shows the average terminal quantities for a period of 30 cycles. Fig. 3.6(a) shows the instantaneous inverter terminal voltage for a duration of 2 cycle and Fig. 3.6(b) shows the inverter firing angle. In this scheme valve 1 is fired after the commutation failure between valves 4 and 6 at the instant when the valve 6 turns off, which for the considered case is instant C' (refer Fig. 3.6(a)). The value of the firing angle at instant C' is $142^{o}$ (refer Fig. 3.6(b)). Valve 2 is then fired at the instant when valves 1 and 4 completely take over the current which results in a firing angle of around $102^{o}$. But valve 2 cannot come into conduction because of the negative voltage across it. This leads to a longer duration of short circuit at the inverter terminal. But with the advanced firing of

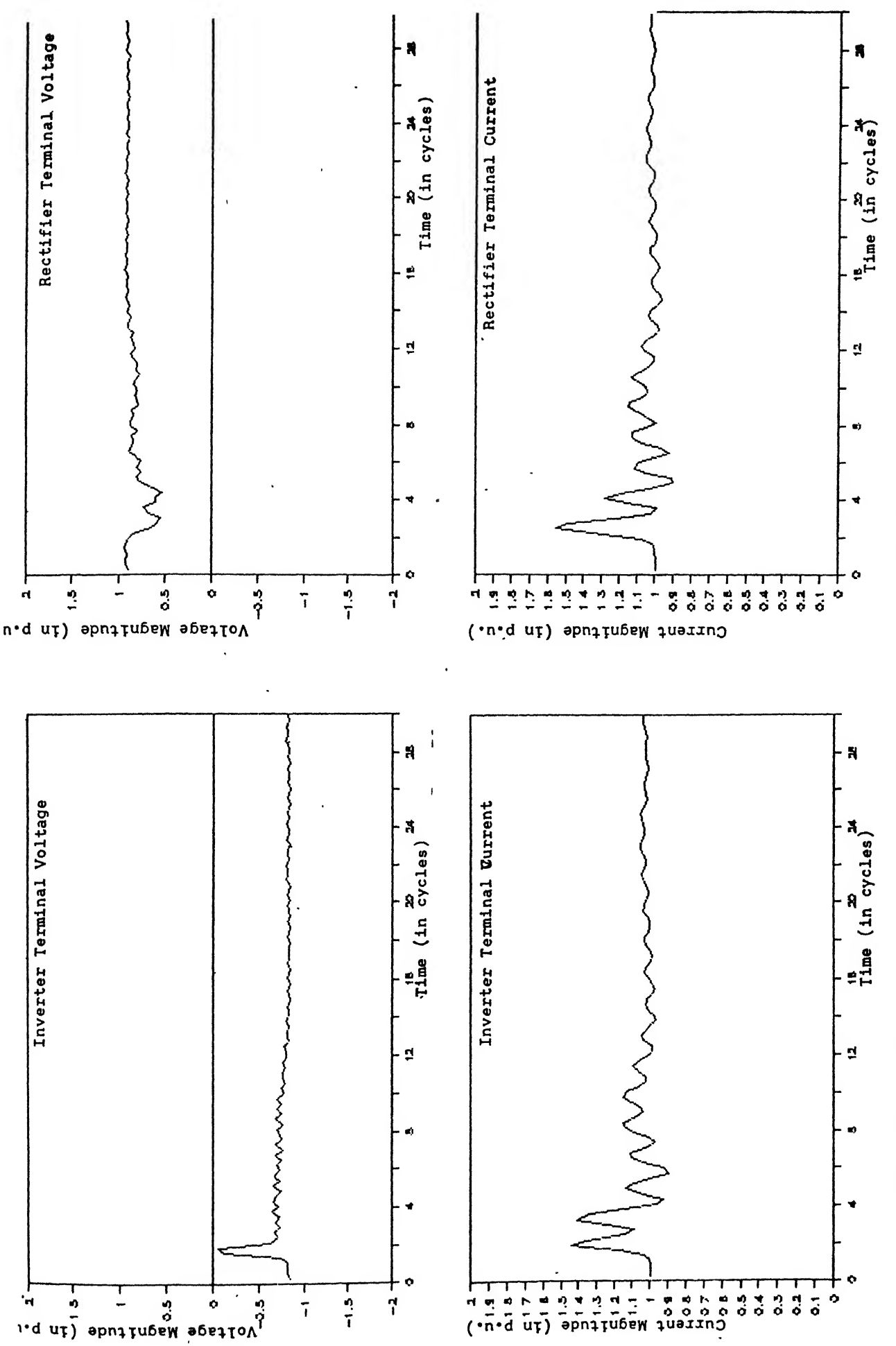



Fig. 3.5 20%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE MODIFICATION IN THE PROPOSED SCHEME

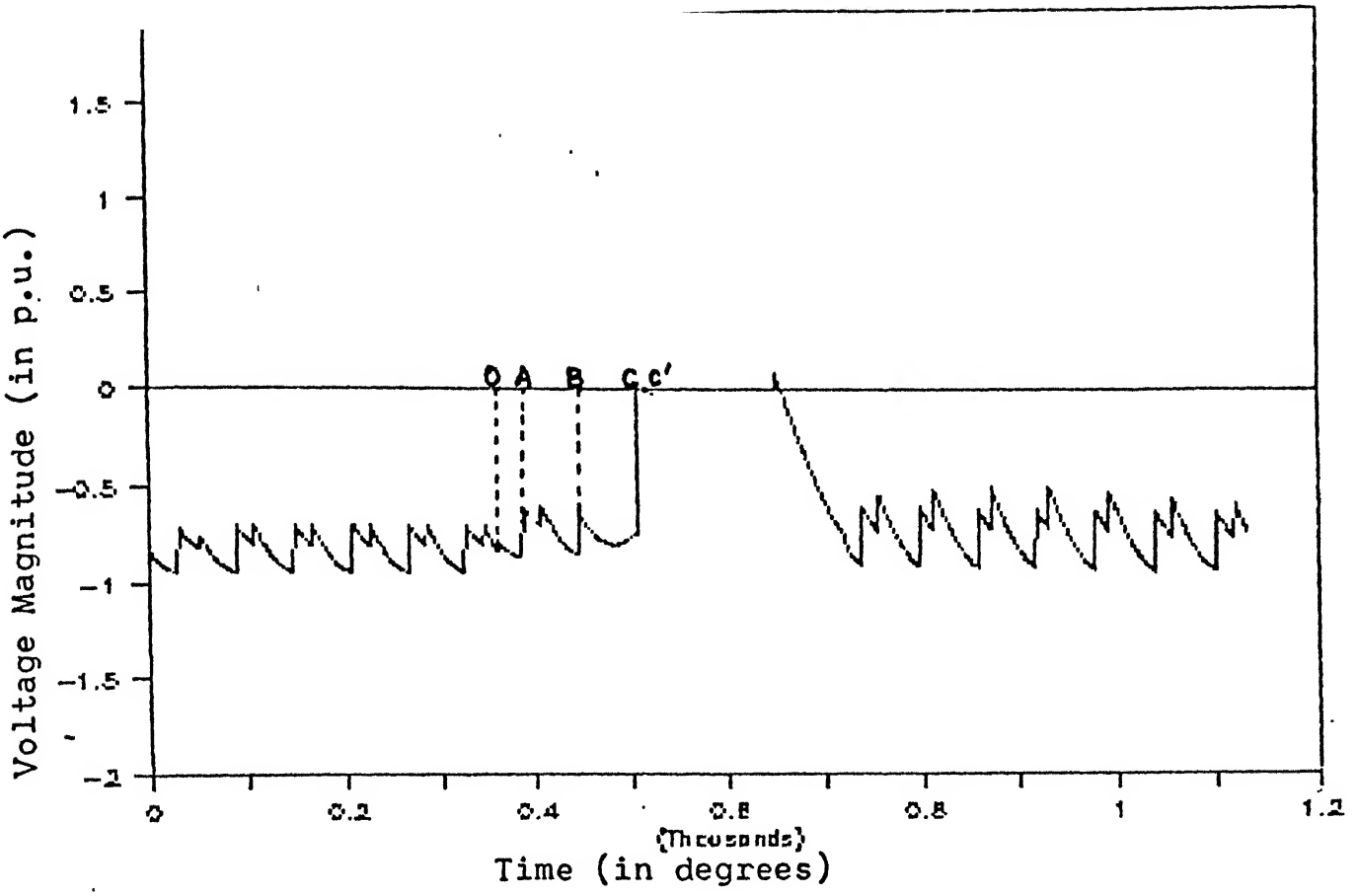



Fig. 3.6(a) INSTANTANEOUS INVERTER TERMINAL VOLTAGE WITH THE MODIFICATION IN THE PROPOSED SCHEME

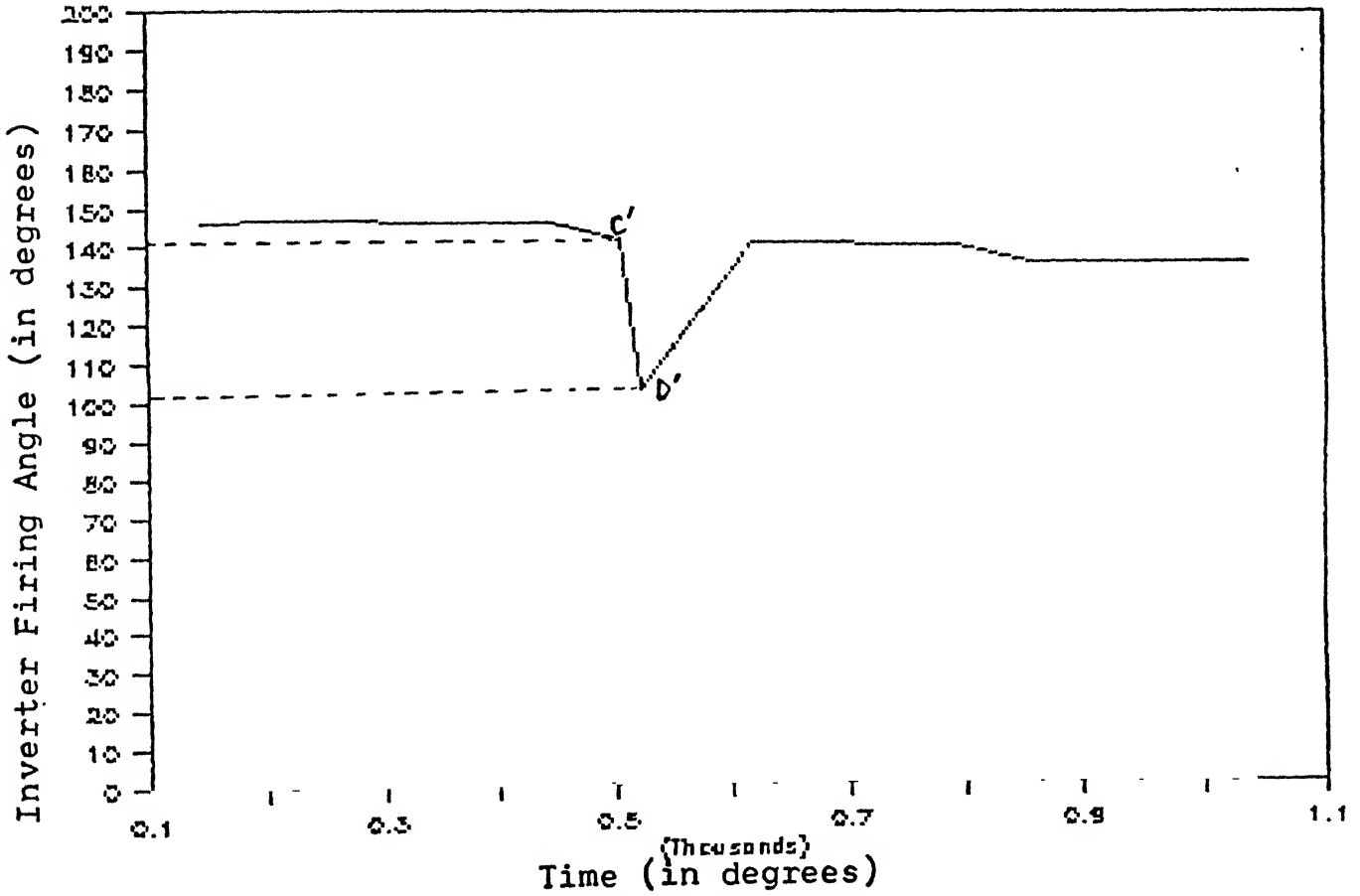
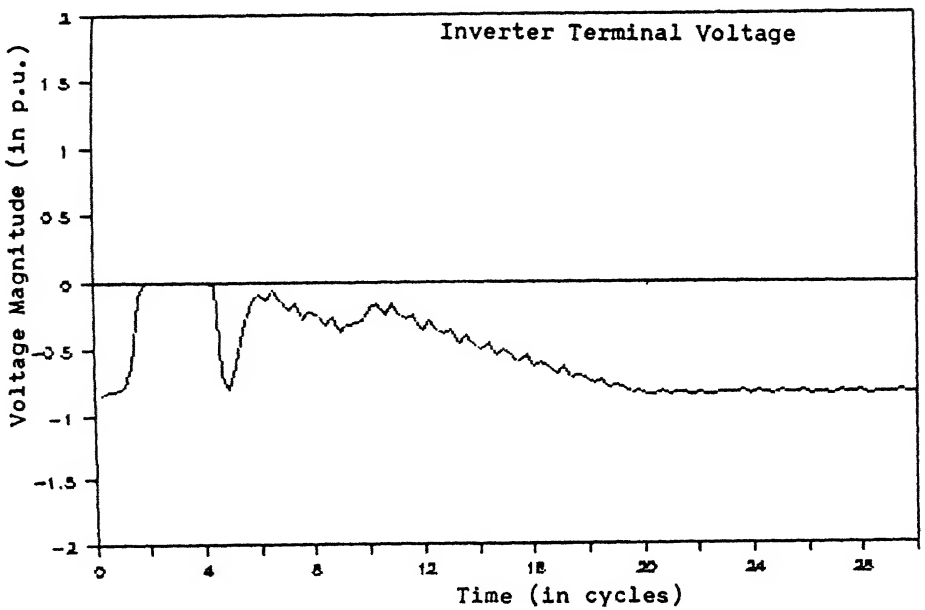


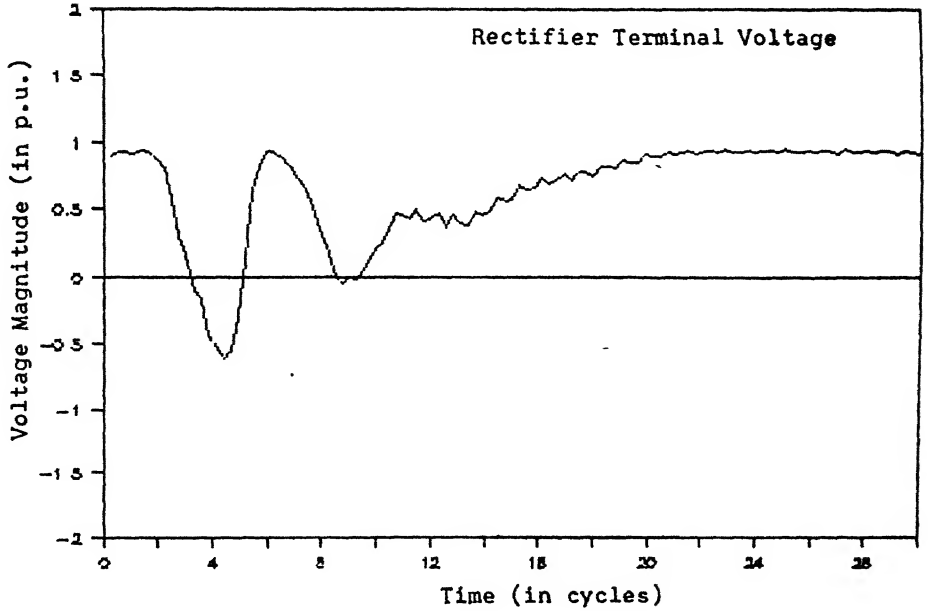

Fig. 3.6(b) INVERTER FIRING ANGLE WITH MODIFICATION IN THE PROPOSED SCHEME

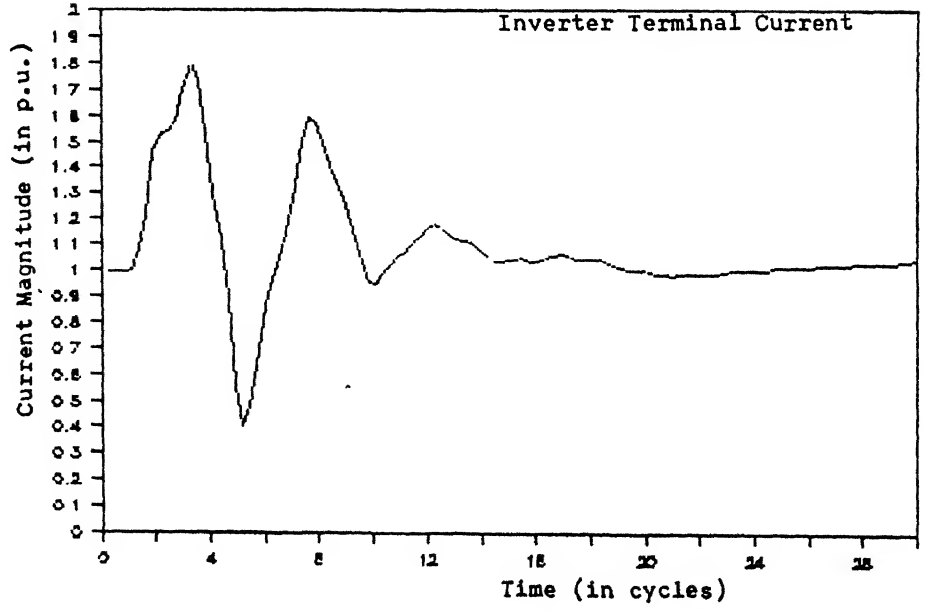
valve 3, further commutation failures are avoided and the system recovers reasonably fast. Hence a comparative study shows that this modified scheme leads to a faster recovery as compared to the normal recovery process but a slower recovery as compared to the proposed recovery scheme. In case B a single cycle 50% dip is considered in phase A inverter voltage. The system response following the considered dip are given in Figs. 3.7 to 3.9. Fig. 3.7 gives the plot for average quantities, viz., average DC terminal voltage and average DC current at both the terminals during normal recovery process. Fig. 3.8 shows the average quantities at both terminals with the proposed recovery scheme and Fig. 3.9 shows the same quantities with modified recovery scheme. It is obvious from these figures that the duration of the short circuit at the inverter terminal has been reduced to a great extent by employing the proposed recovery scheme. However, the positive voltage at the inverter terminal for a short duration is the price of using proposed recovery scheme. With the modification suggested previously, the voltage at the inverter terminal doesn't become positive but it remains at a smaller value for a comparatively longer duration.

The current waveform has the smallest peak with the proposed recovery scheme but has subsequent oscillations of small magnitude. Rectifier terminal voltage response has also improved considerably with the proposed recovery scheme.

The fault considered in case C is a single cycle 99% dip in phase A voltage at inverter terminal. The system response



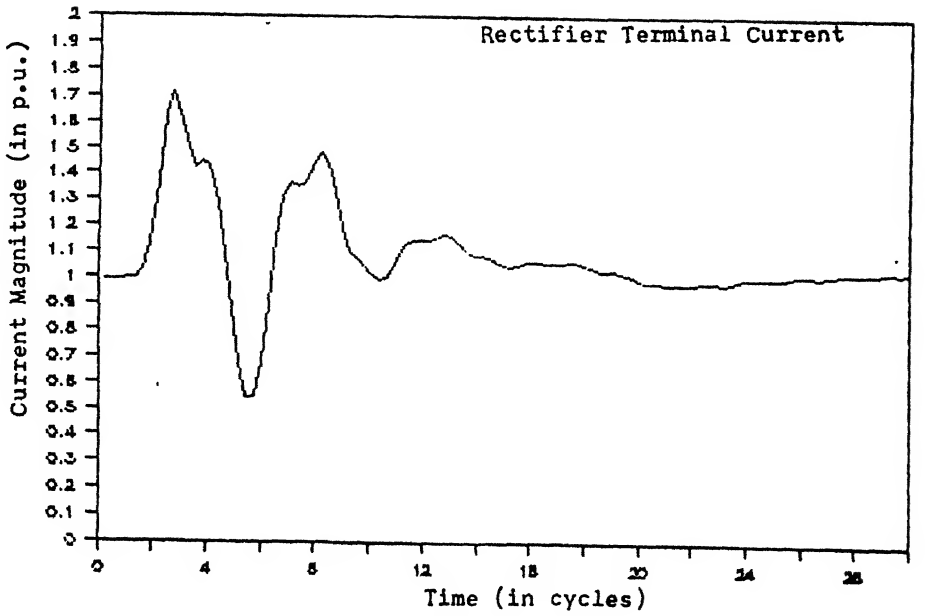
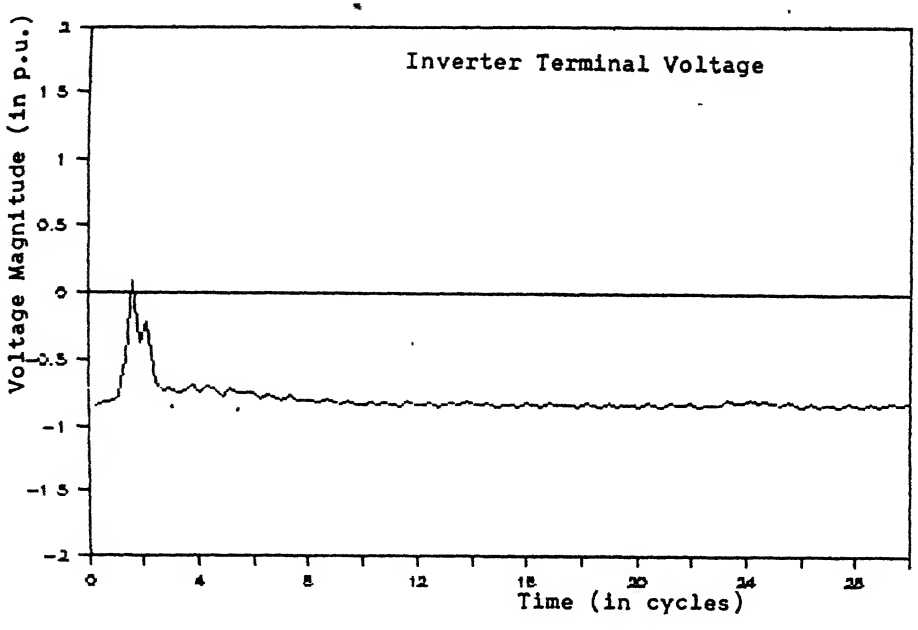
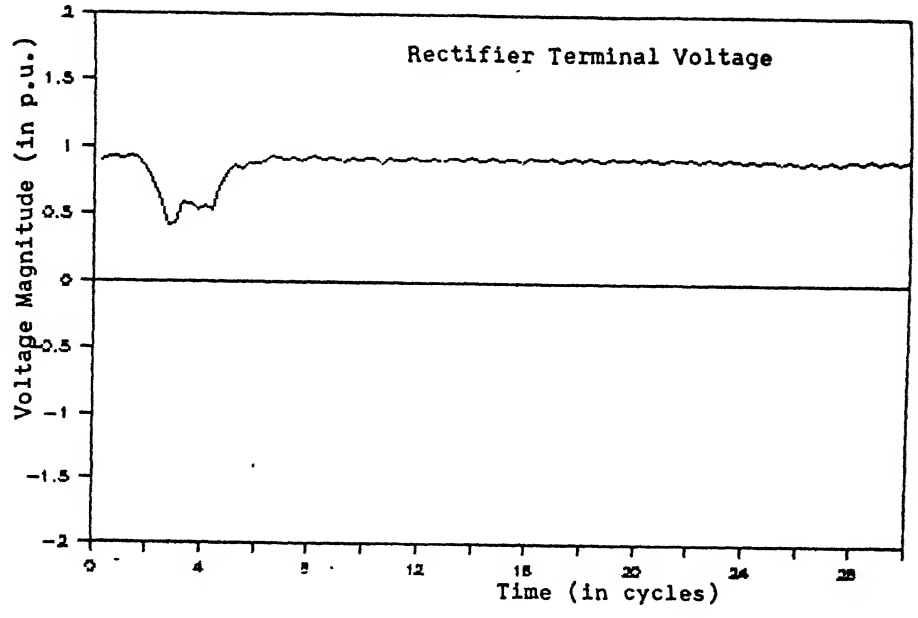
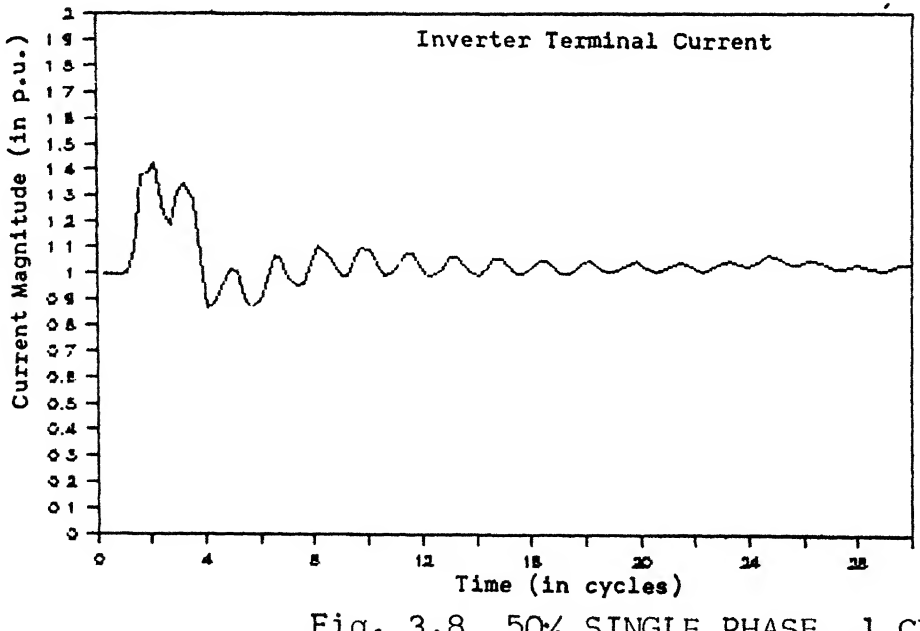




Fig. 3.7 50%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER,NORMAL RECOVERY



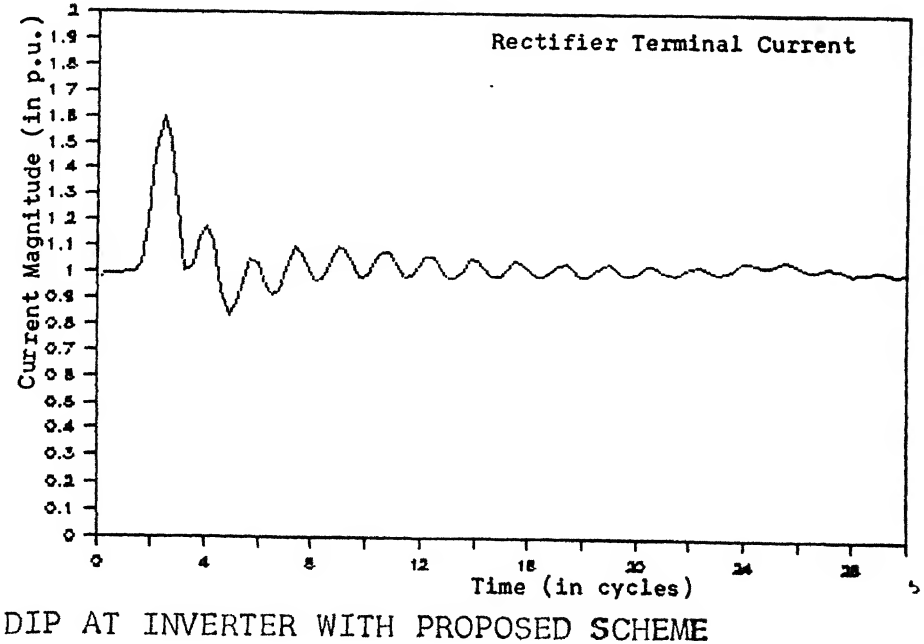
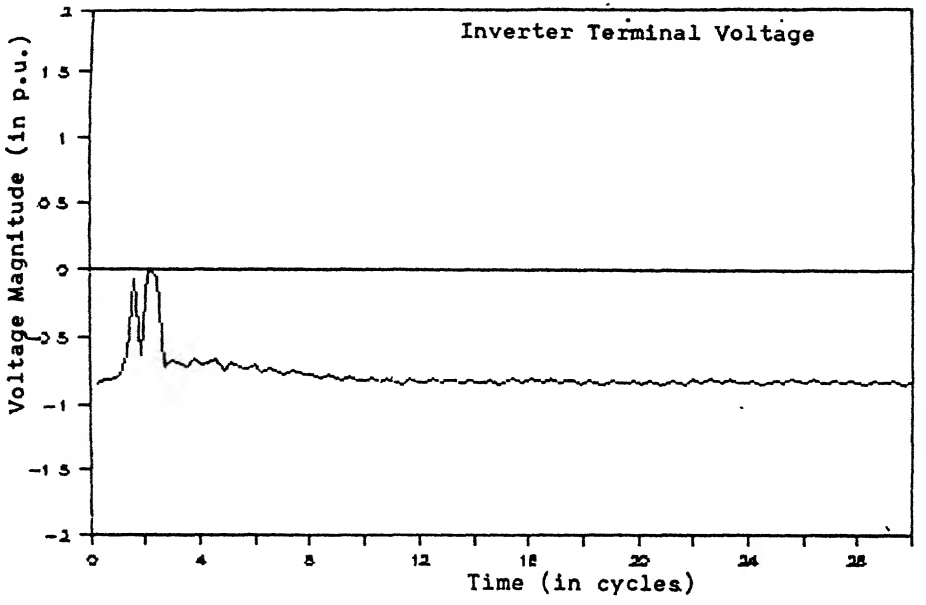
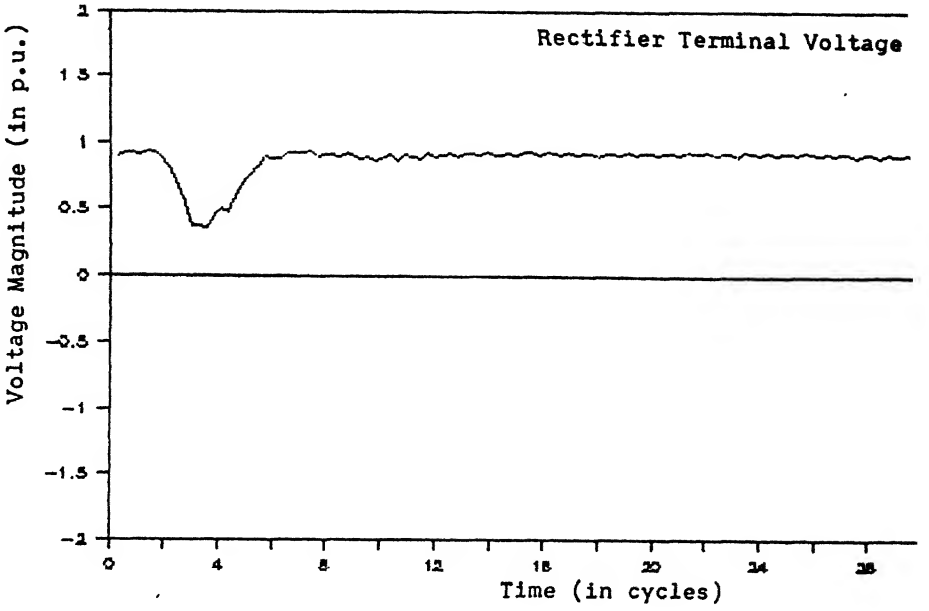
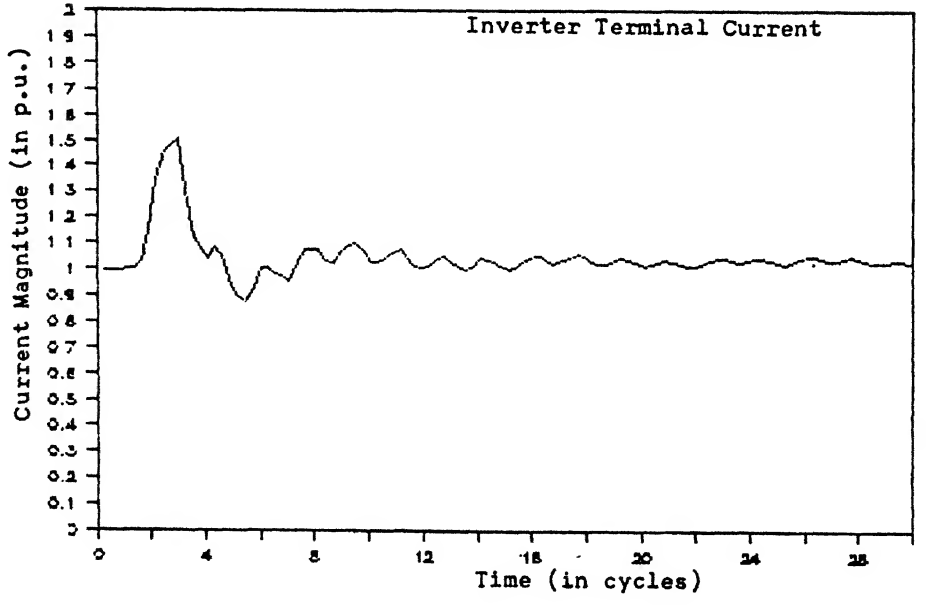




Fig. 3.8 50% SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH PROPOSED SCHEME



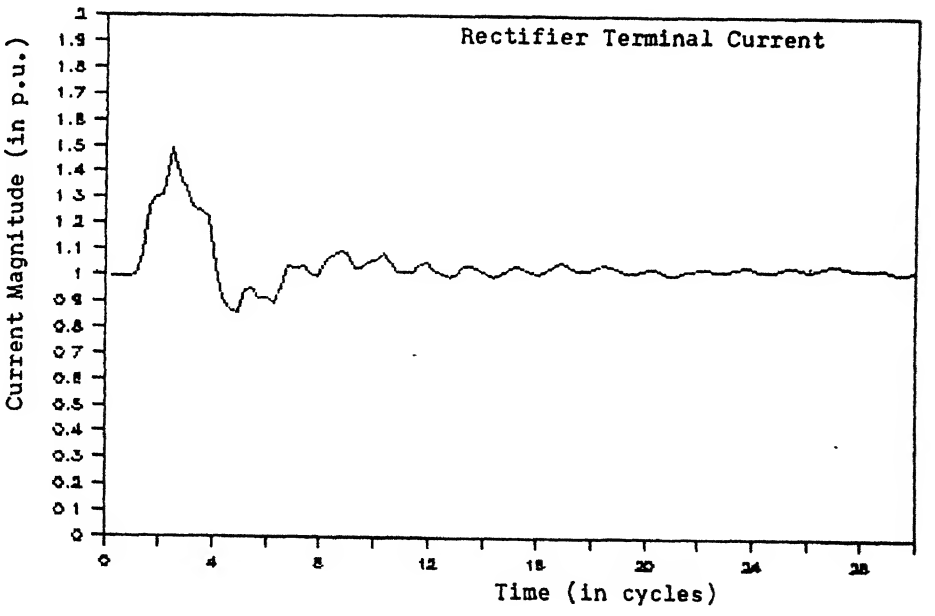



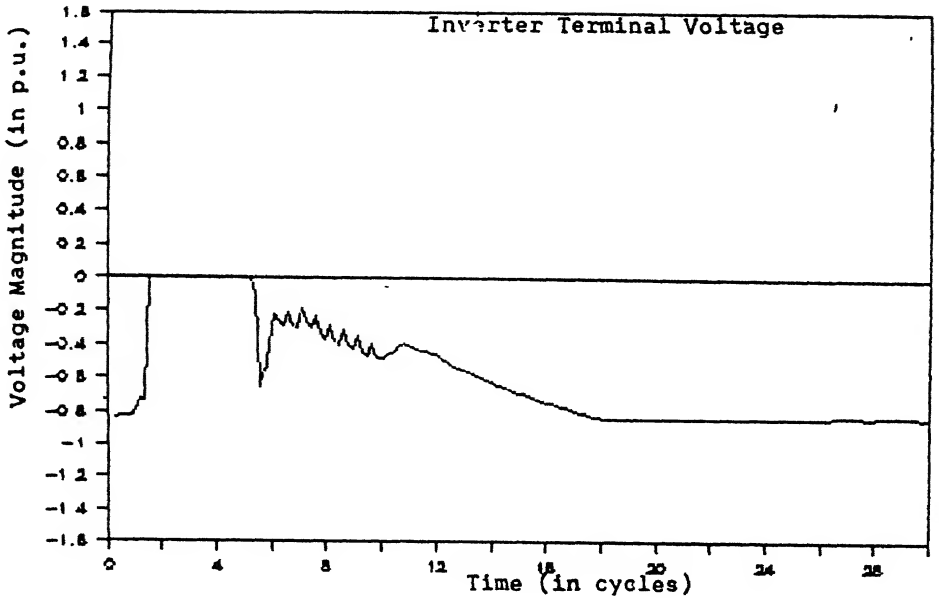

Fig. 3.9 50%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER
WITH MODIFICATION IN THE PROPOSED SCHEME

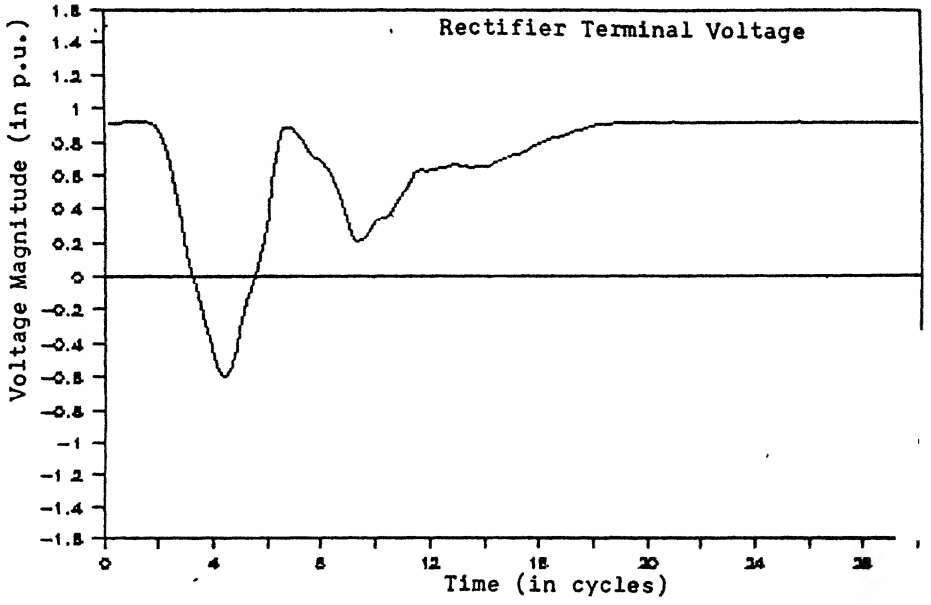
following this fault is shown in Figs. 3.10 to 3.12. Fig. 3.10 shows the behaviour of the system following a momentary single phase collapse without any forced firing. Fig. 3.11 shows the system response with the proposed recovery scheme and Fig. 3.12 shows the recovery process with the modification in the proposed scheme. It is evident from the above figures that the recovery scheme has improved the response to a great extent by reducing the duration of the short circuit across the inverter terminal. The current waveform has the oscillations with the low peak value. The advance of the firing angle is illustrated in Figs. 3.13 and 3.14. Fig. 3.13(a) shows the instantaneous inverter terminal voltage and Fig. 3.13(b) shows the variation in the inverter firing angle with proposed recovery scheme and Fig. 3.14(a) and (b) shows the same plots with the modification in the proposed scheme. It is obvious from these figures that there is a forced firing of valves in the rectifier region to provide them sufficient margin to complete the commutation thereby improving the system response.

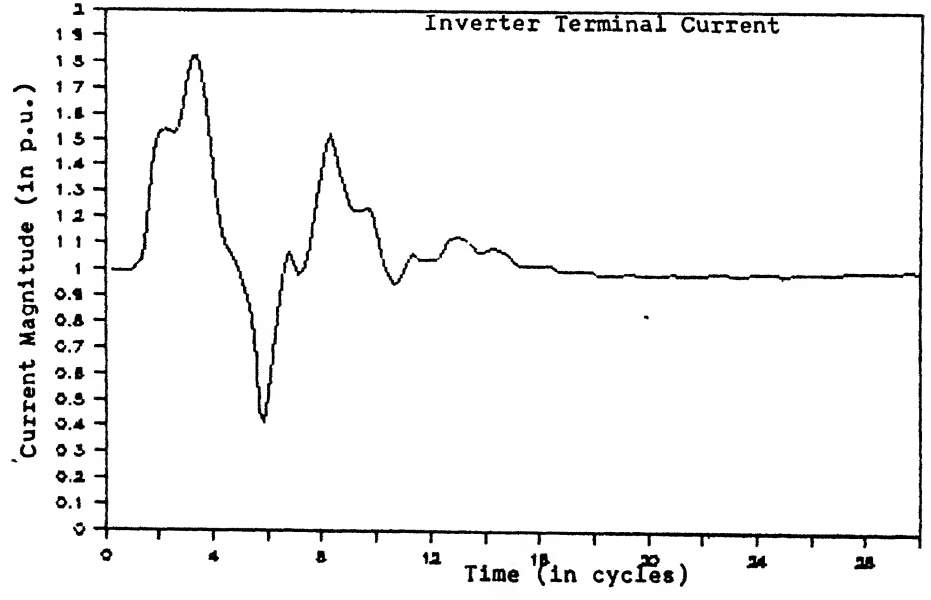
Based on the above case studies it is evident that the proposed scheme improves the system recovery to a great extent following single phase short duration faults.

### 3.4.2 Prolonged Single Phase to Ground Faults

In this section the following faults are considered :



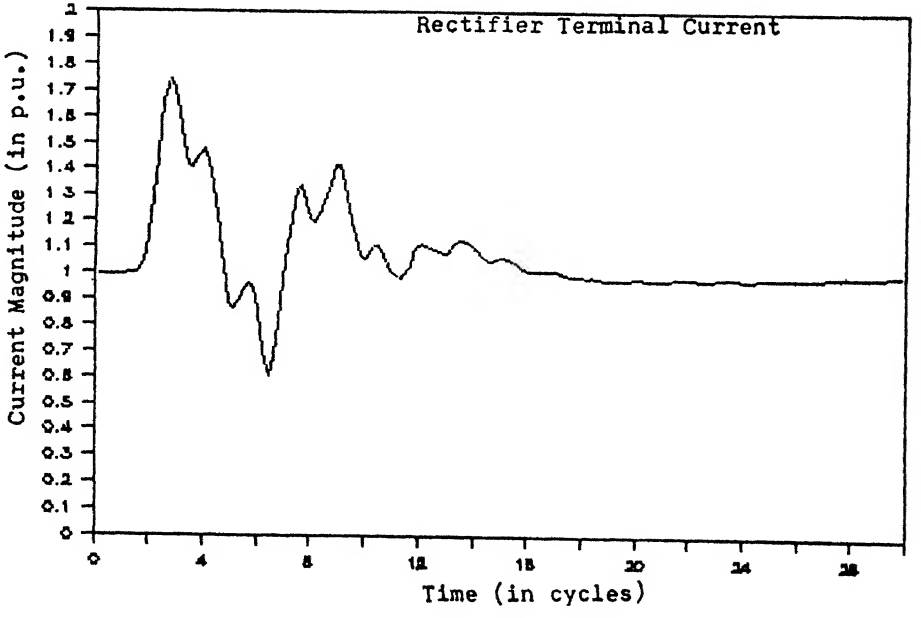
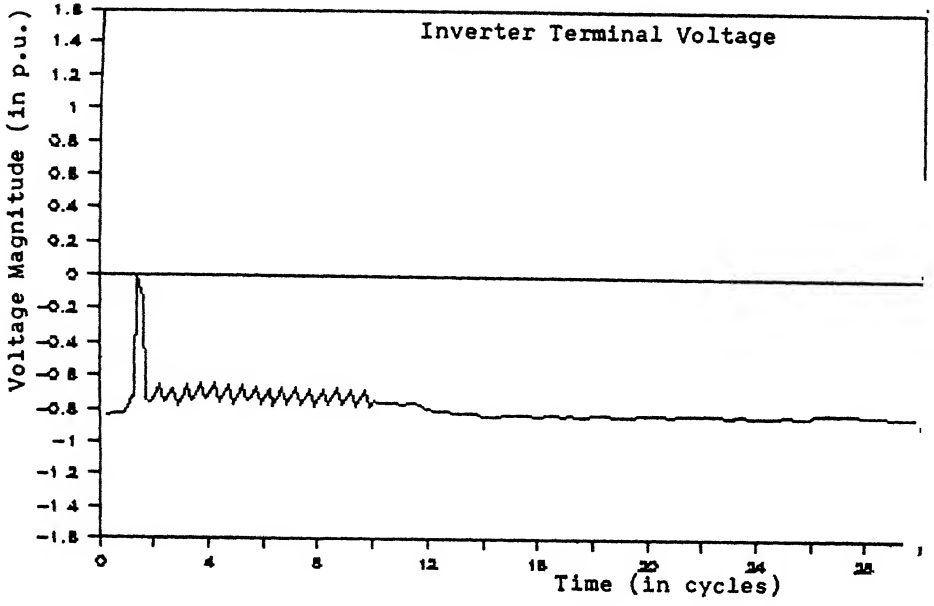
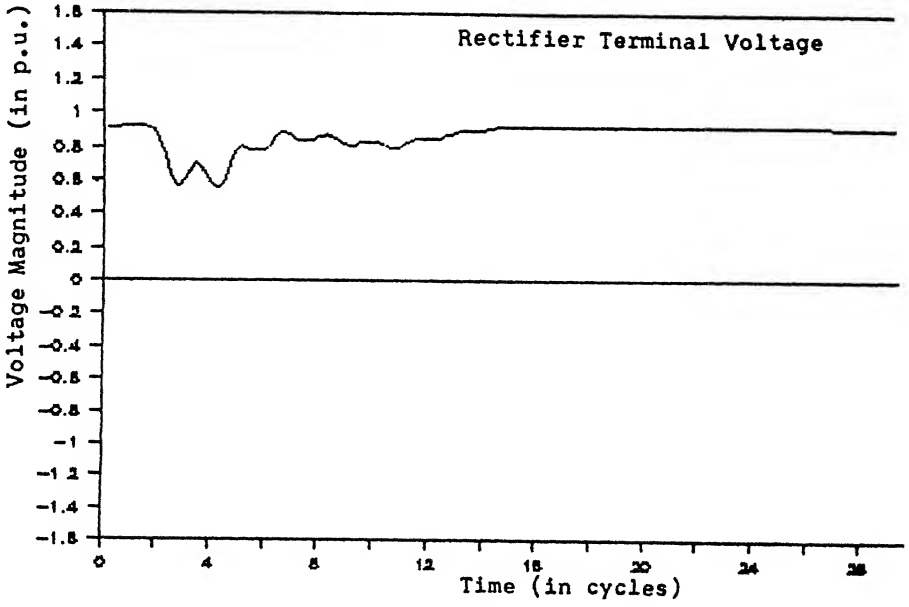
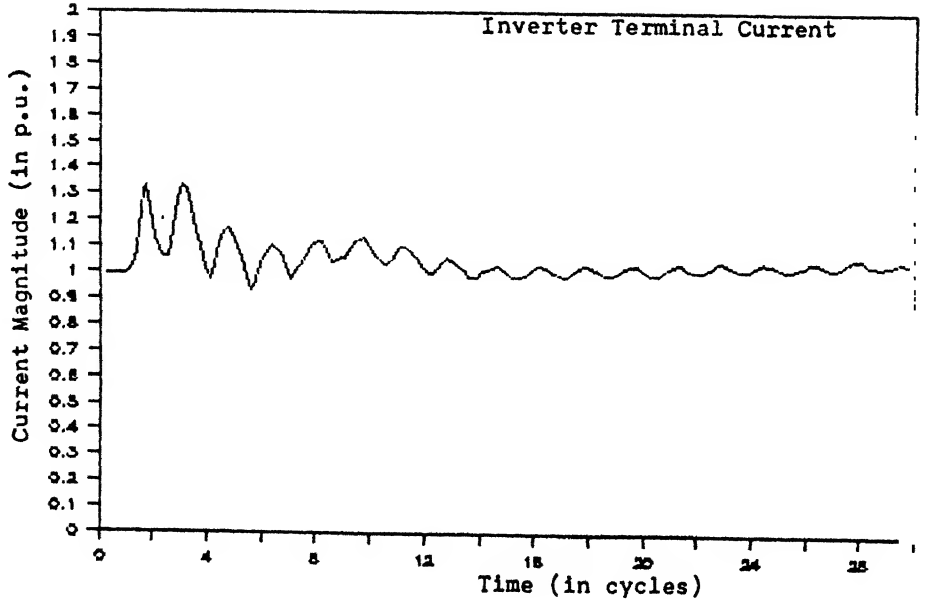




Fig. 3.10 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER
NORMAL RECOVERY



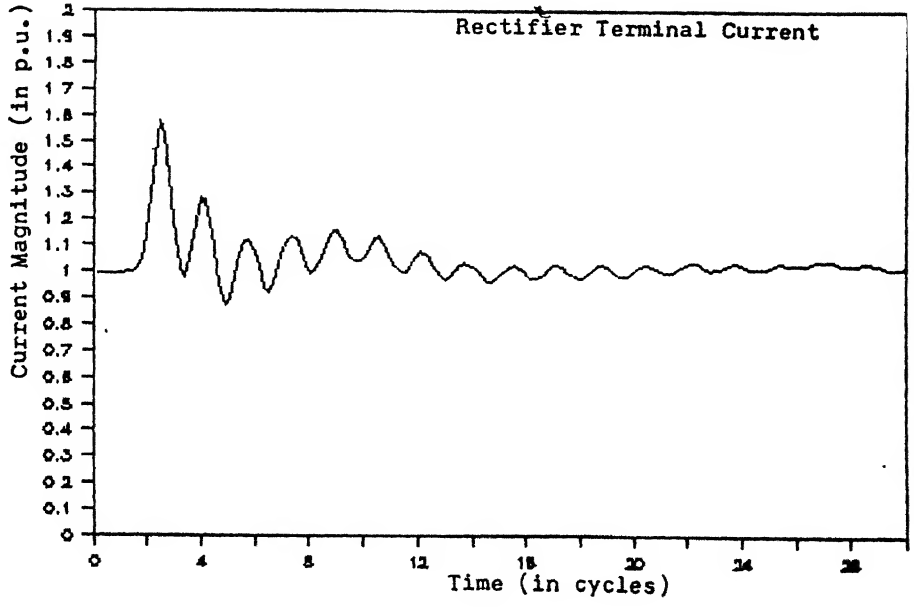
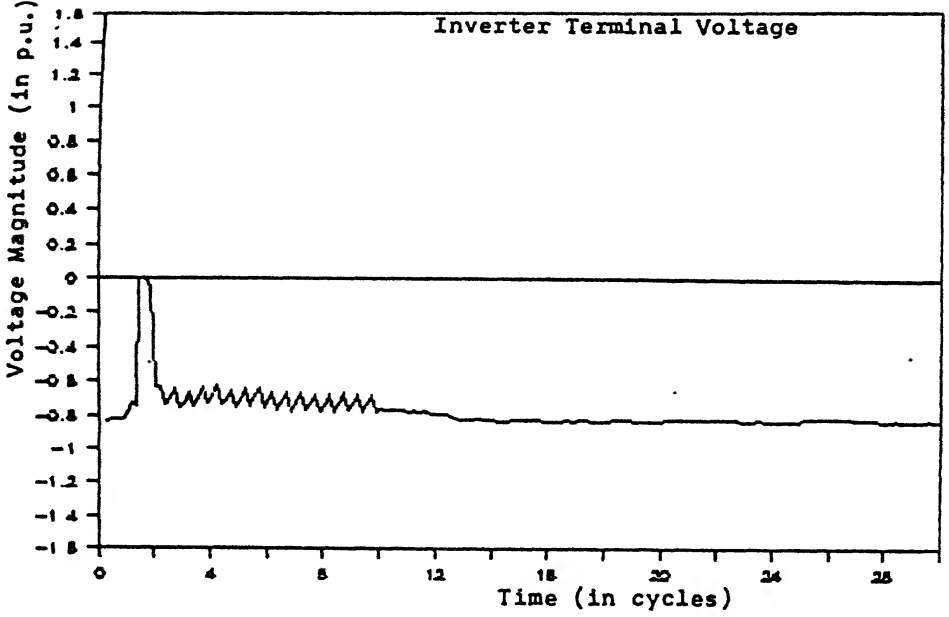
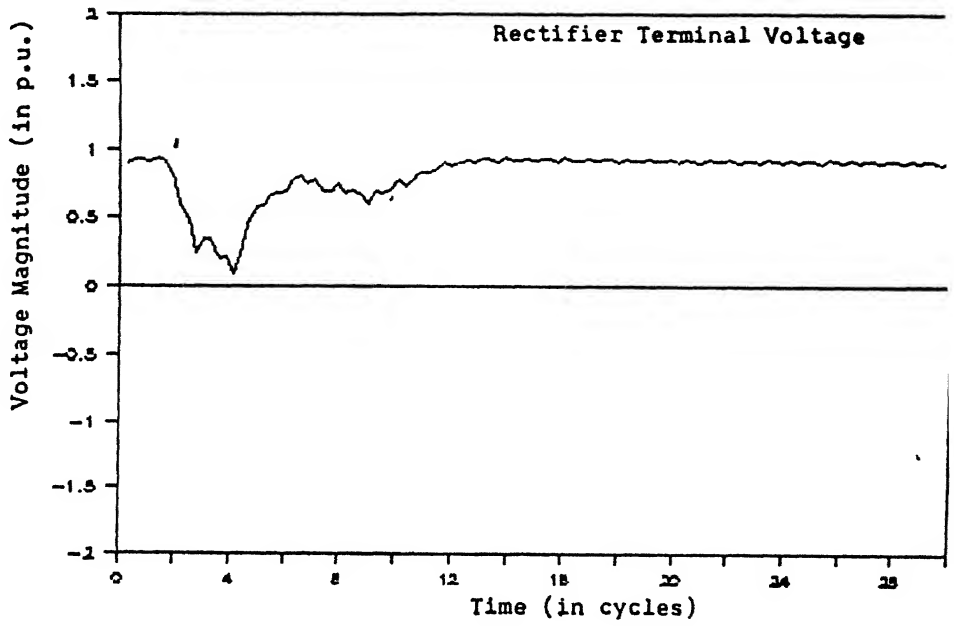
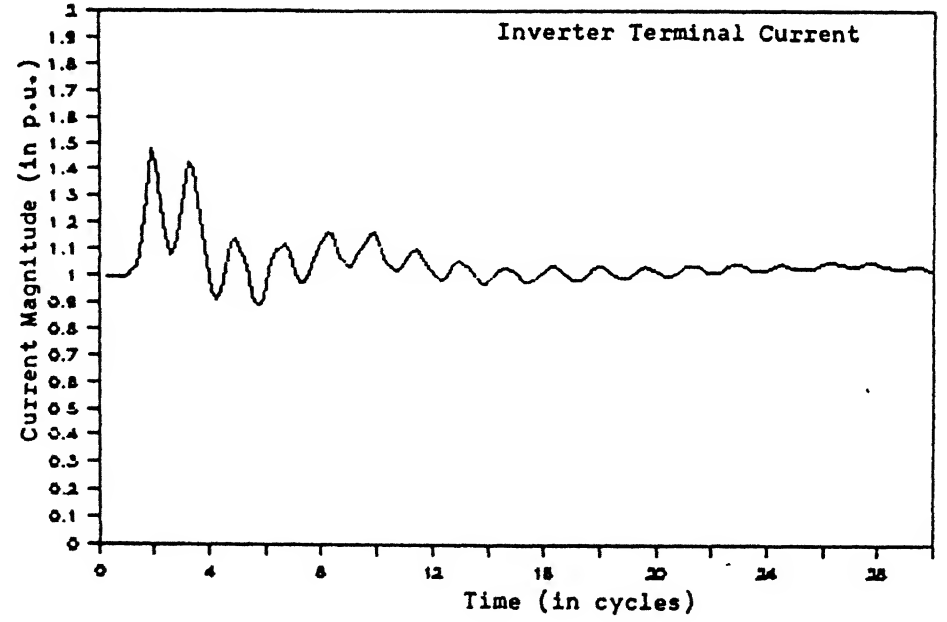




Fig. 3.11 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



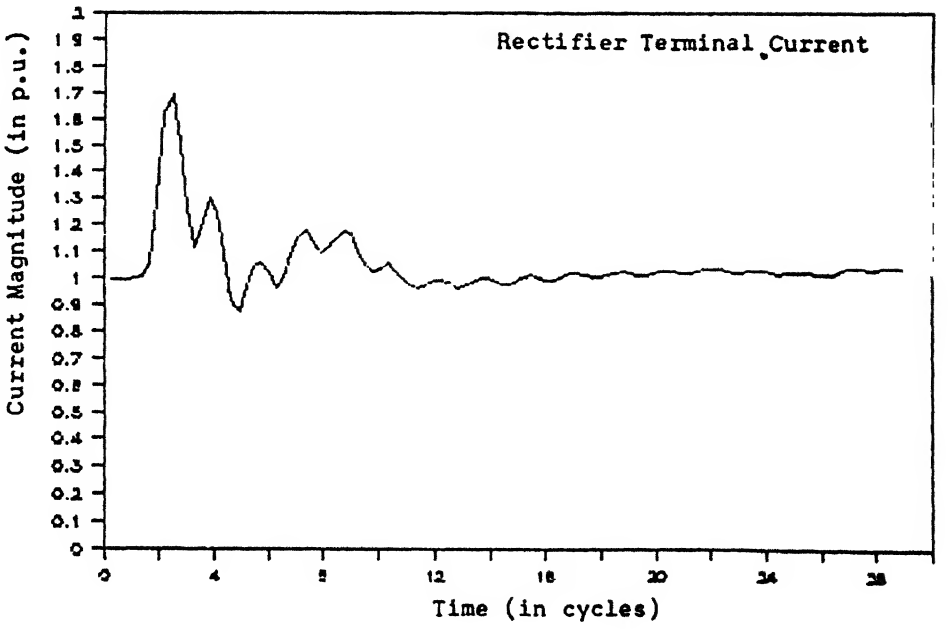




Fig. 3.12 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH MODIFICATION IN THE PROPOSED SCHEME

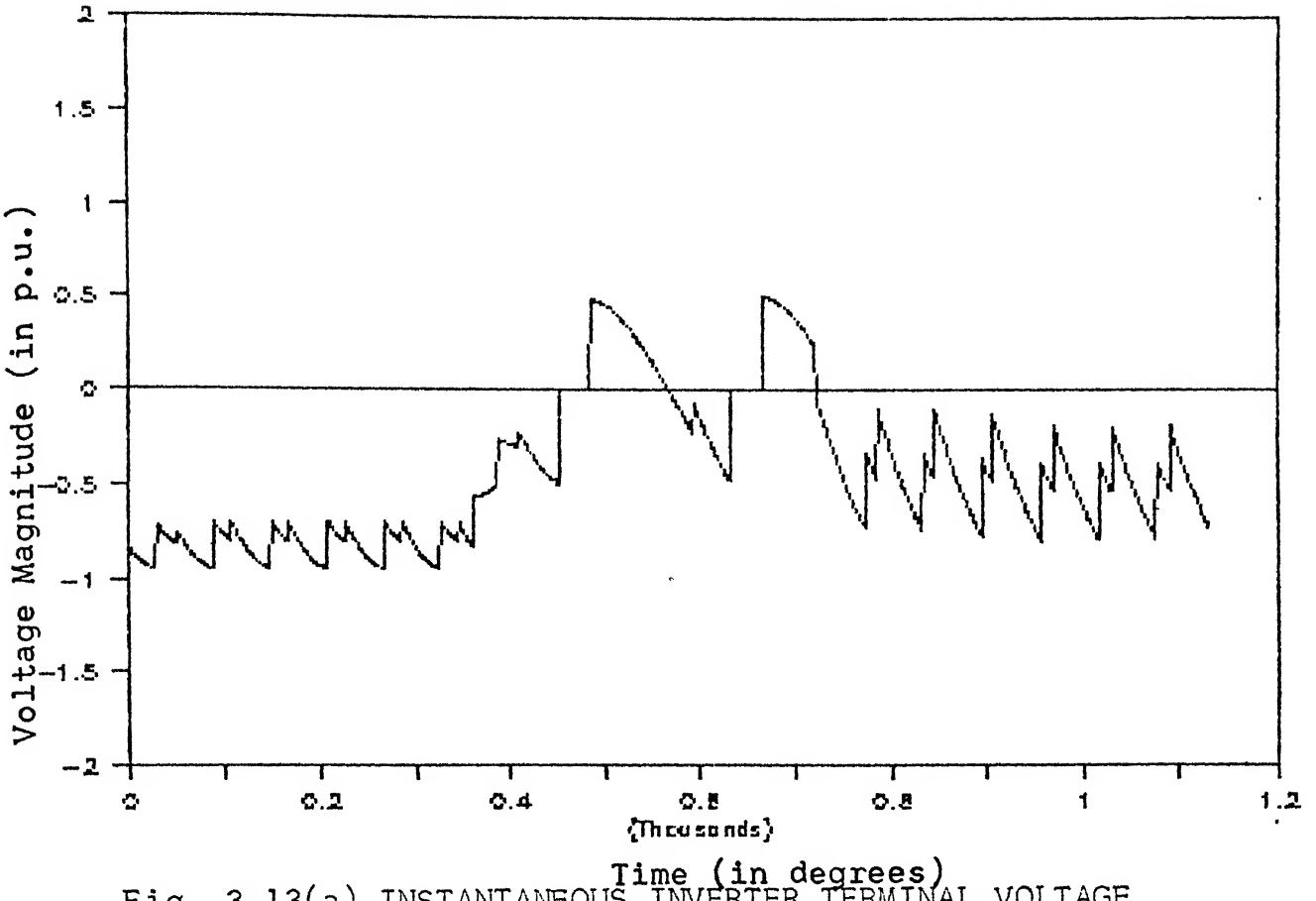



Fig. 3.13(a) INSTANTANEOUS INVERTER TERMINAL VOLTAGE WITH THE PROPOSED SCHEME

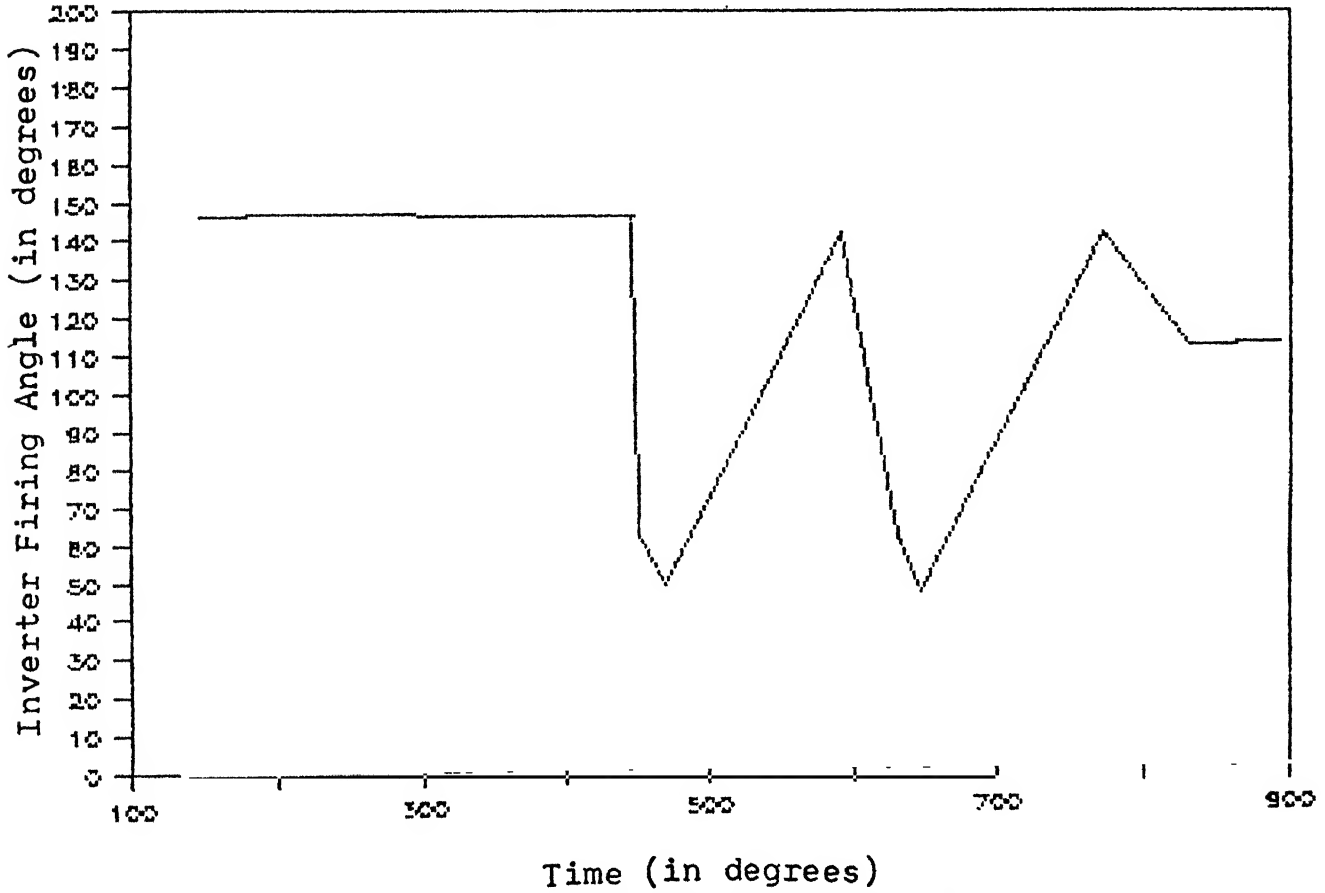



Fig. 3.13(b) INVERTER FIRING ANGLE WITH THE PROPOSED SCHEME

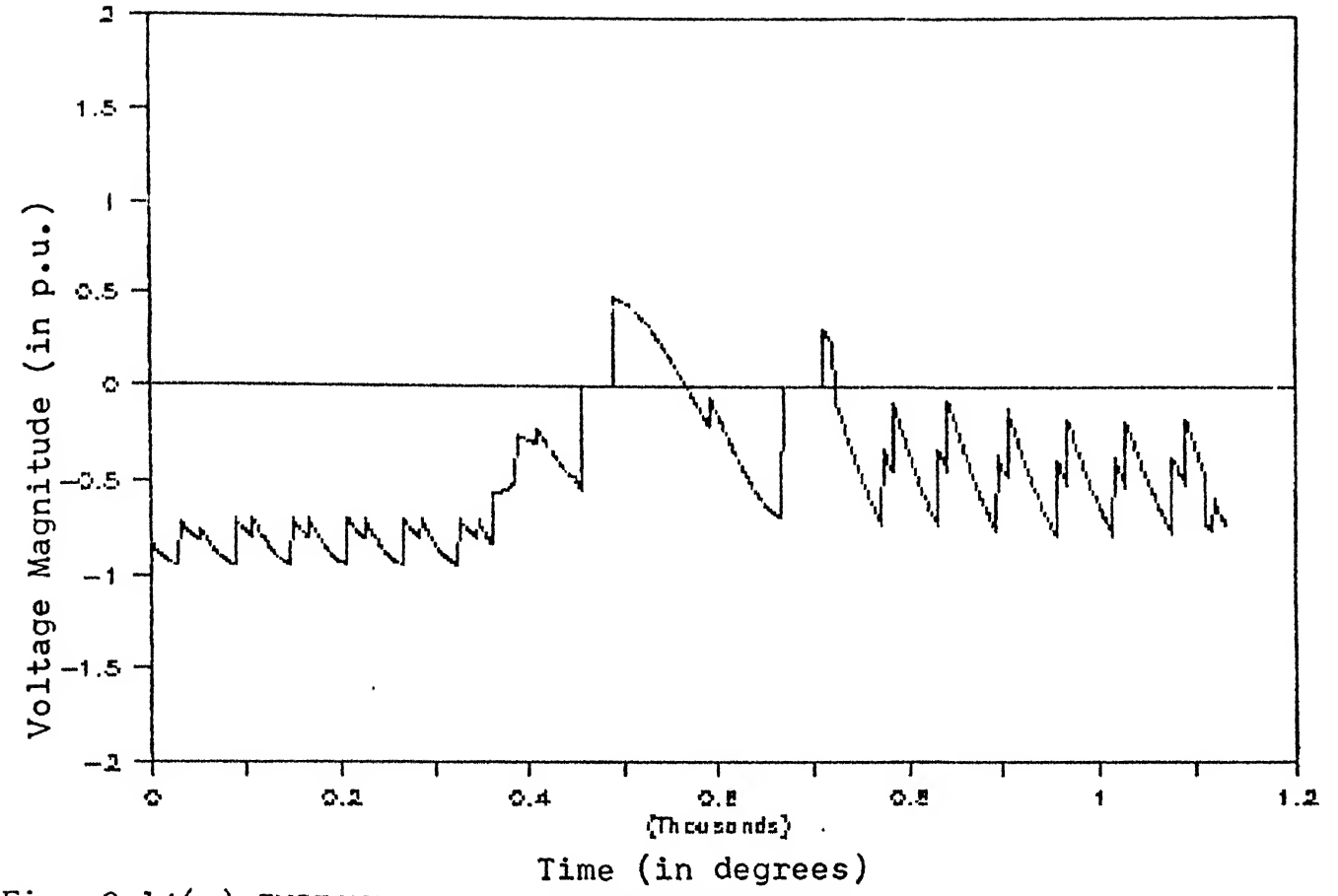



Fig. 3.14(a) INSTANTANEOUS INVERTER TERMINAL VOLTAGE WITH MODIFICATION IN THE PROPOSED SCHEME

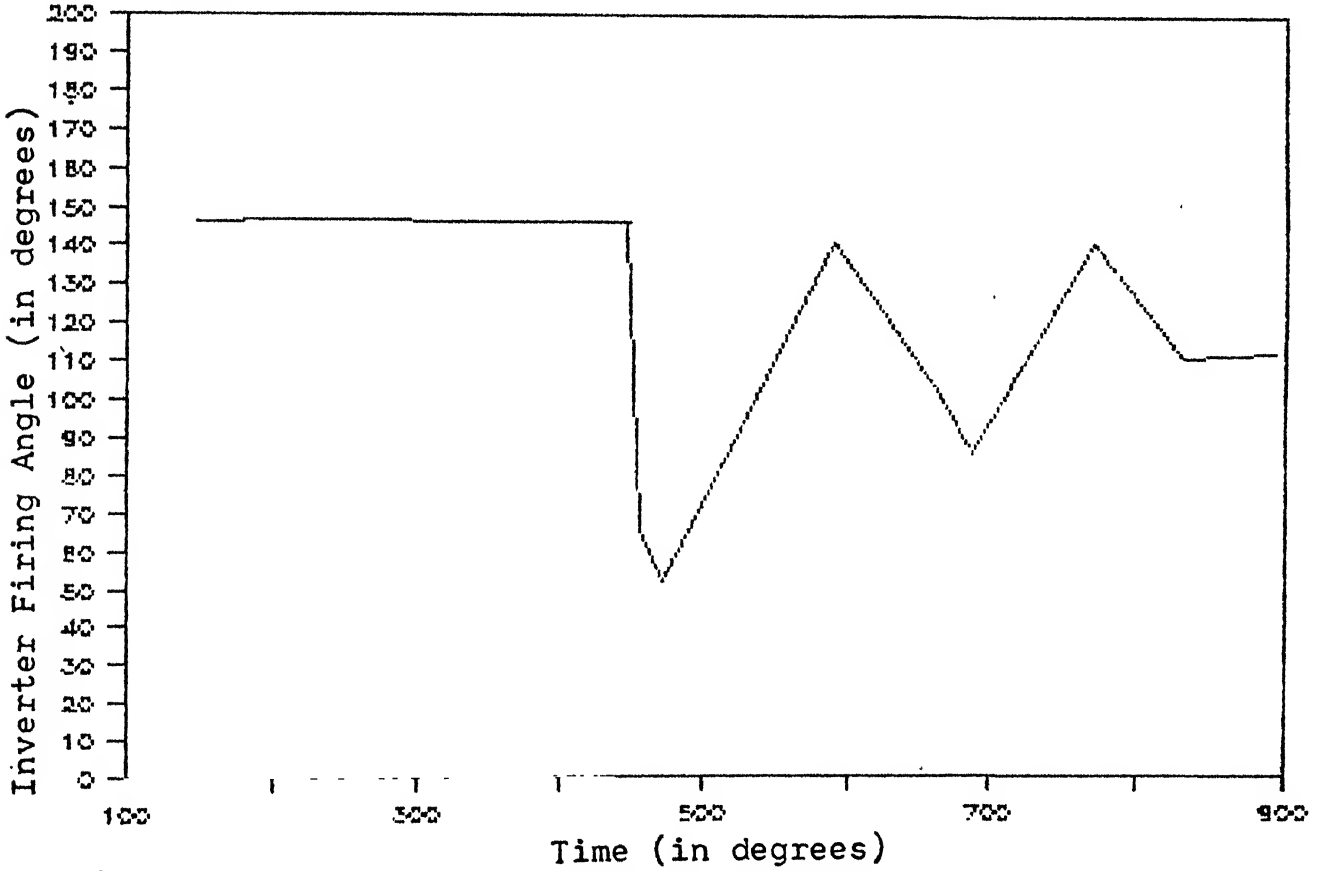


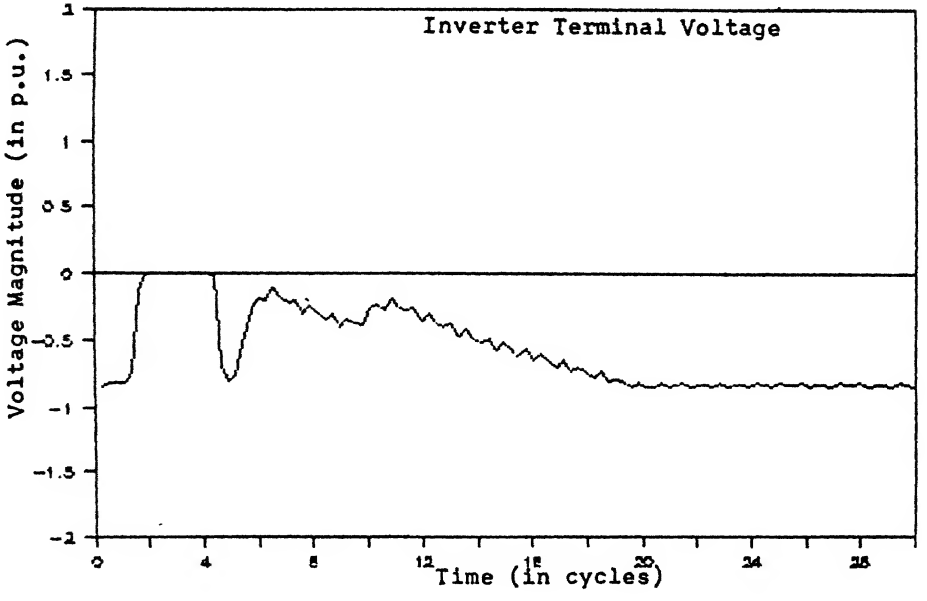

Fig. 3.14(b) INVERTER FIRING ANGLE WITH MODIFICATION IN THE PROPOSED SCHEME

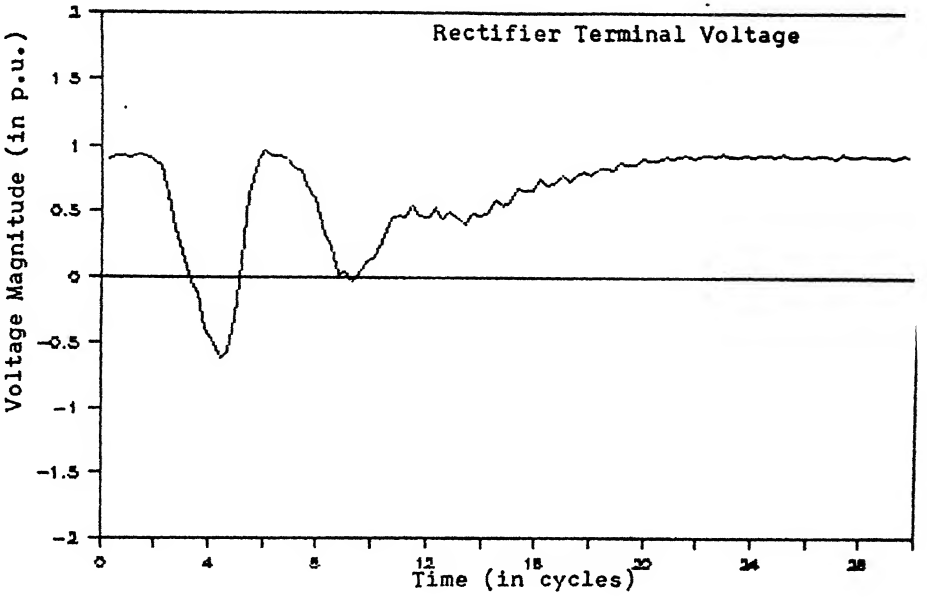
(a) 10 cycle, 20% dip in phase A voltage

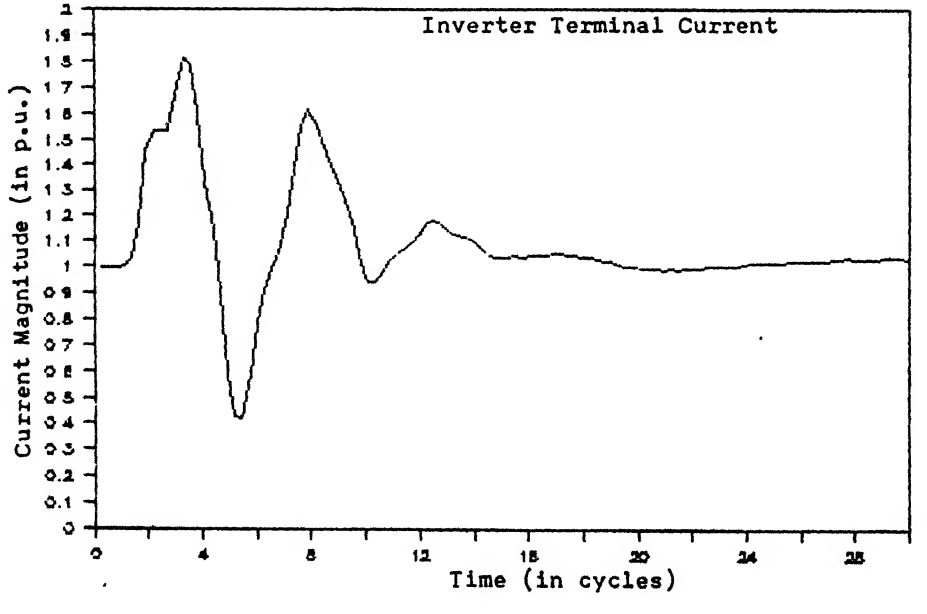
(b) 10 cycle, 50% dip in phase A voltage

(c) 10 cycle, 99% dip in phase A voltage.

For the fault considered in phase A, the system response is reported in Figs. 3.15 to 3.17. Fig. 3.15 shows the system response with normal recovery process and Figs. 3.16 and 3.17 shows the system recovery with proposed recovery scheme and with the modification considered. It is evident from Fig. 3.15 that system starts recovering even in the presence of the fault with normal recovery process because, with the reduced value of link current inverter switches over to current control and facilitates recovery. However, a comparative study of all the figures show the superiority of the proposed scheme over the normal recovery process. Oscillations in the current and rectifier voltage waveforms during the fault are reduced to smaller peak values with the proposed recovery scheme. However, following the recovery, slight oscillations can be noticed in the current waveform. System response to the fault considered in case B are reported in Figs. 3.18 to 3.20. From Fig. 3.18 which shows the system response with normal recovery process, it is evident that the short circuit at the inverter terminal persists for the whole duration of the dip, whereas, with the proposed recovery scheme this duration has been reduced to a great extent and system starts recovering even in the presence



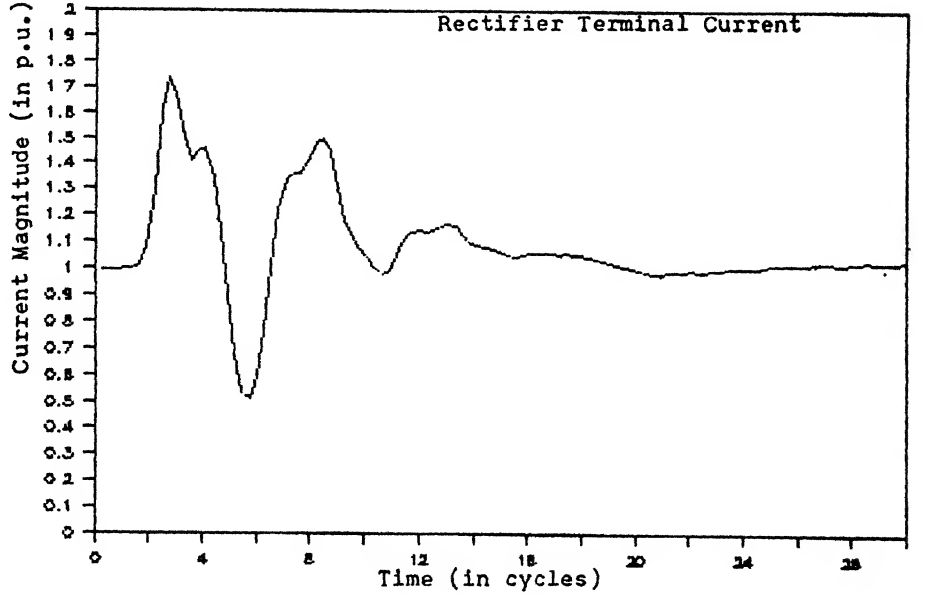




Fig. 3.15 20%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY

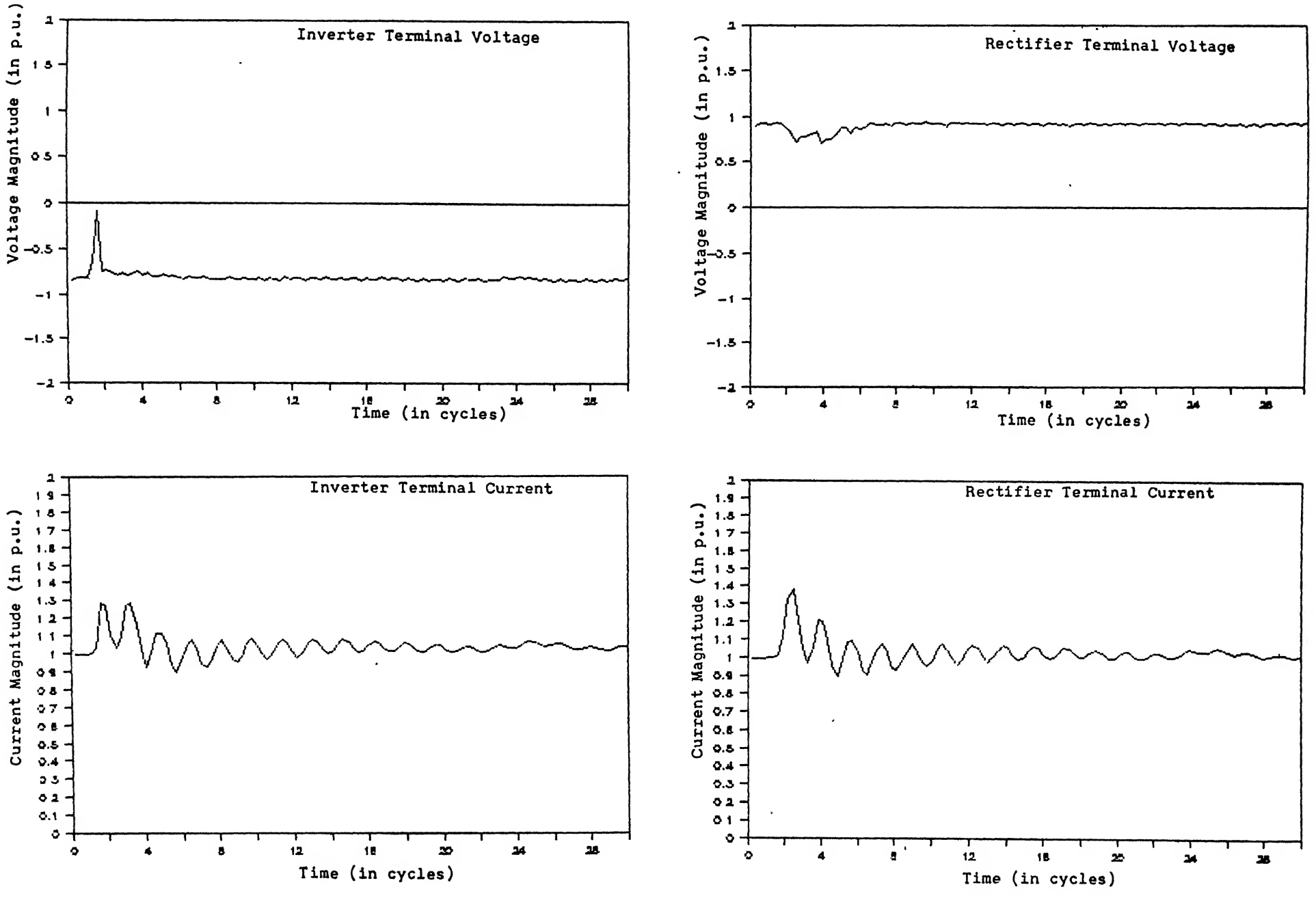
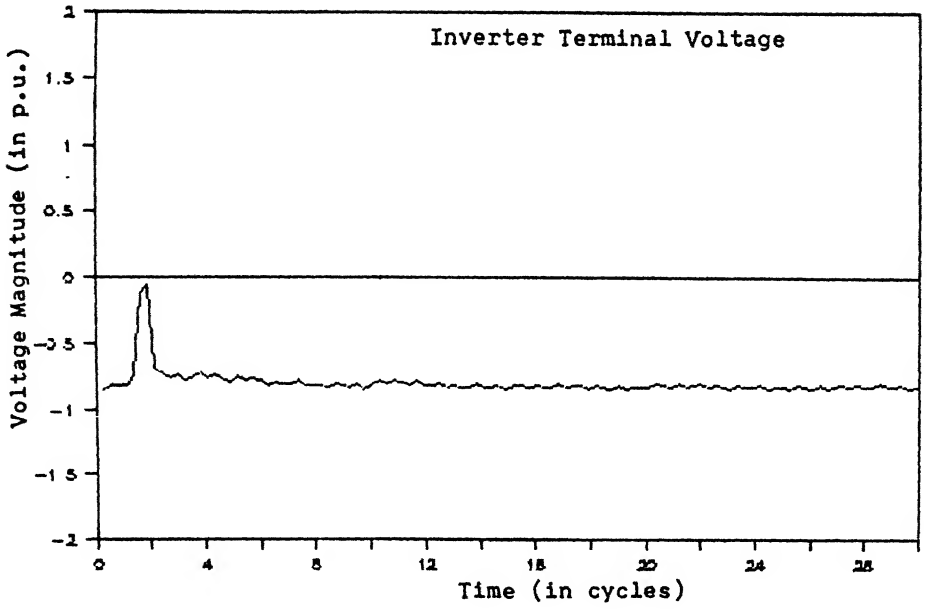
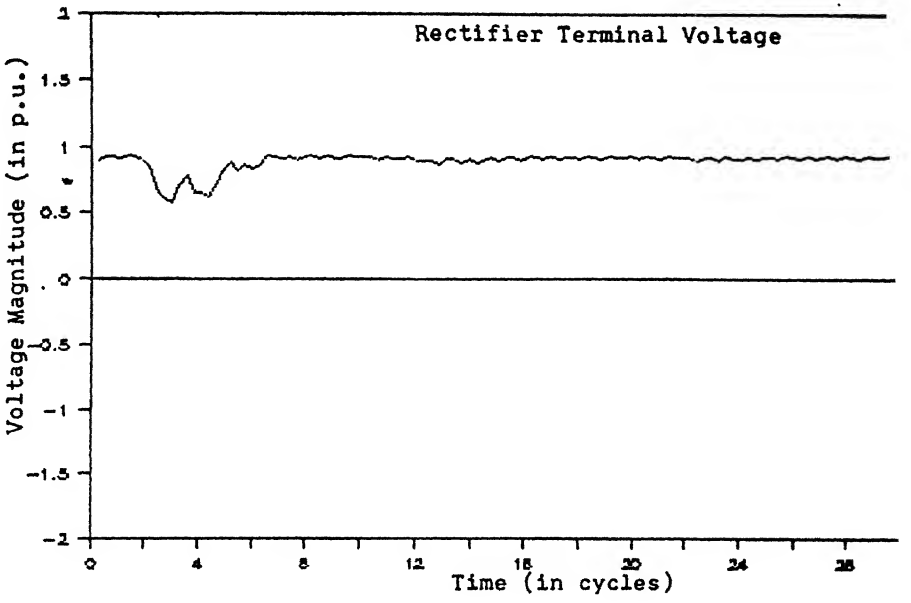
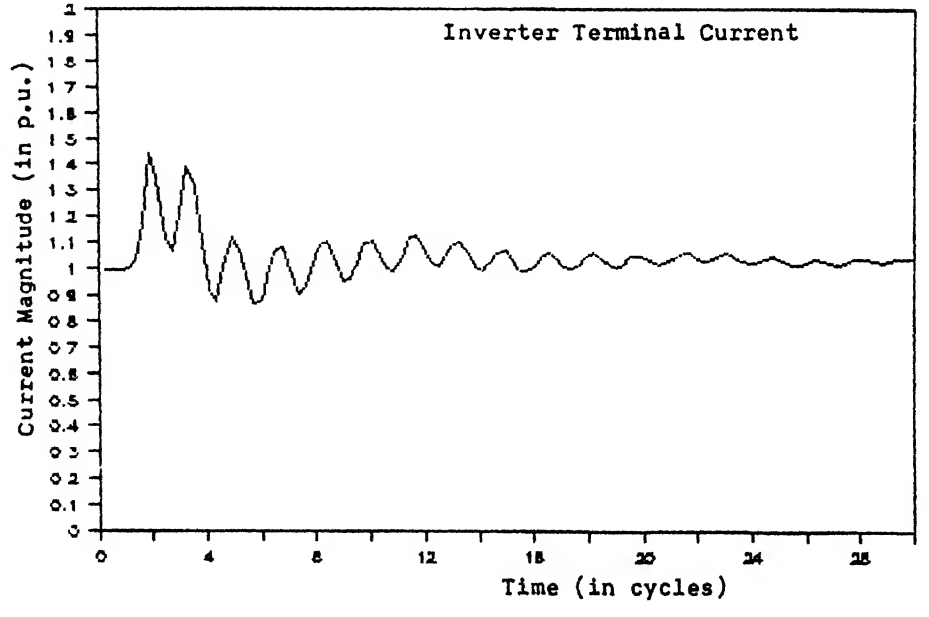



Fig. 3.16 20%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH PROPOSED RECOVERY SCHEME



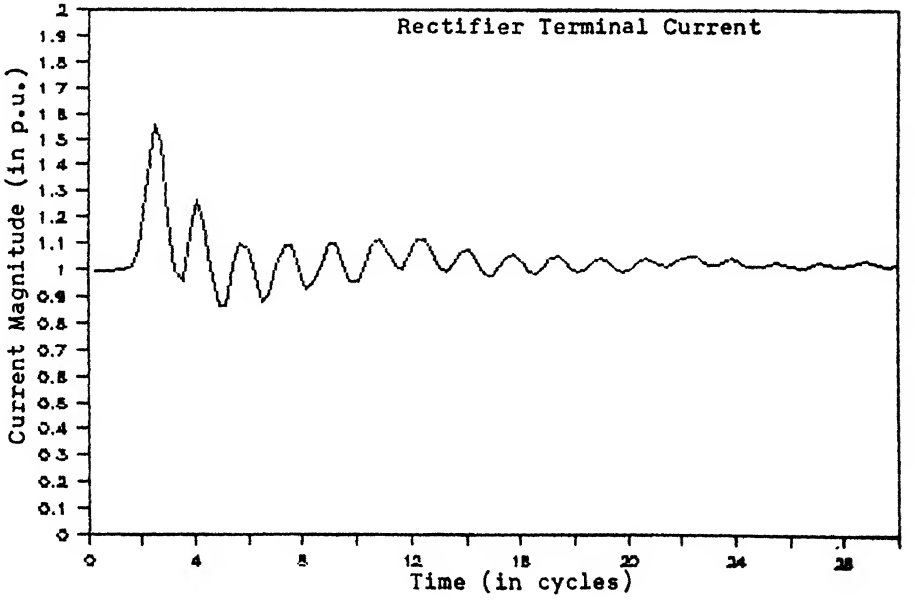
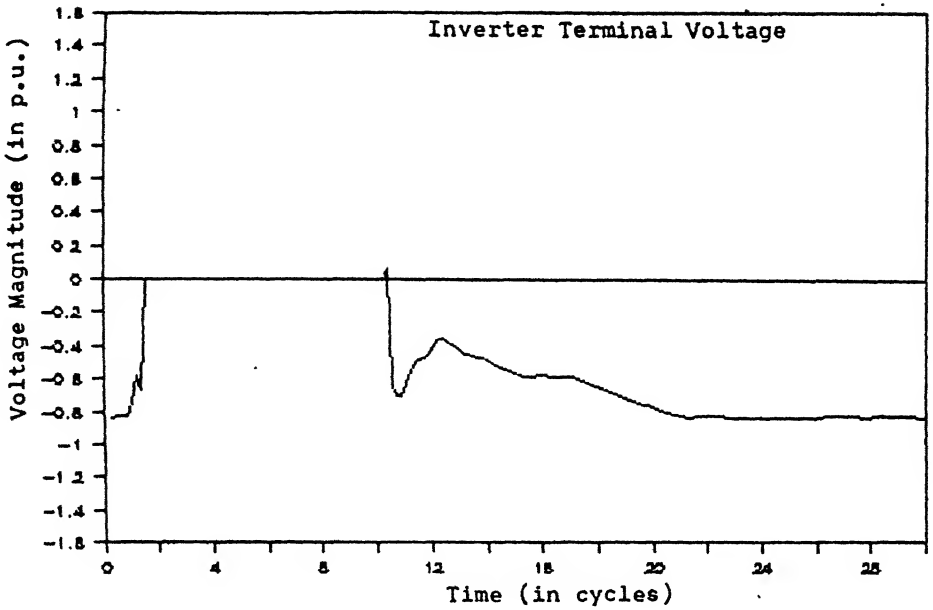
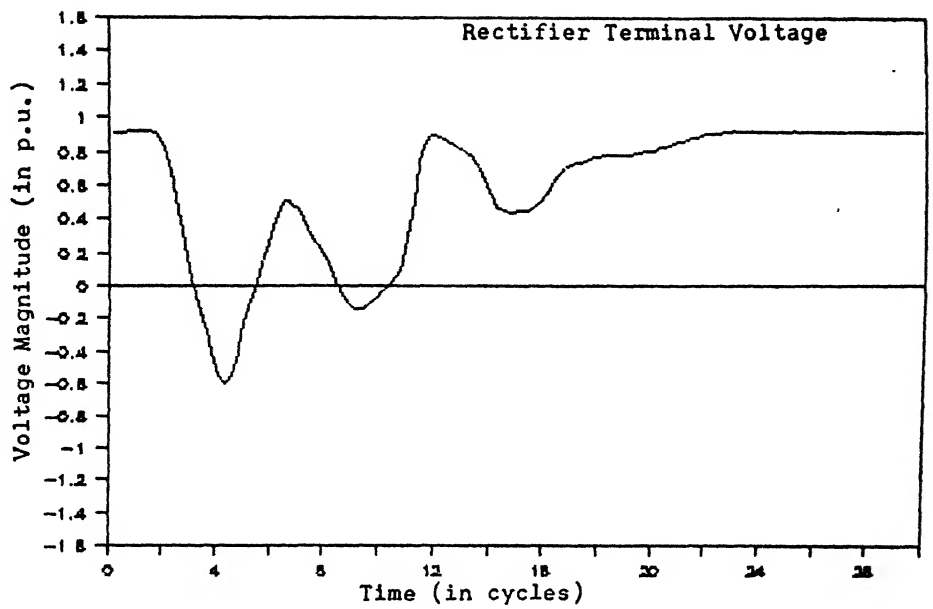
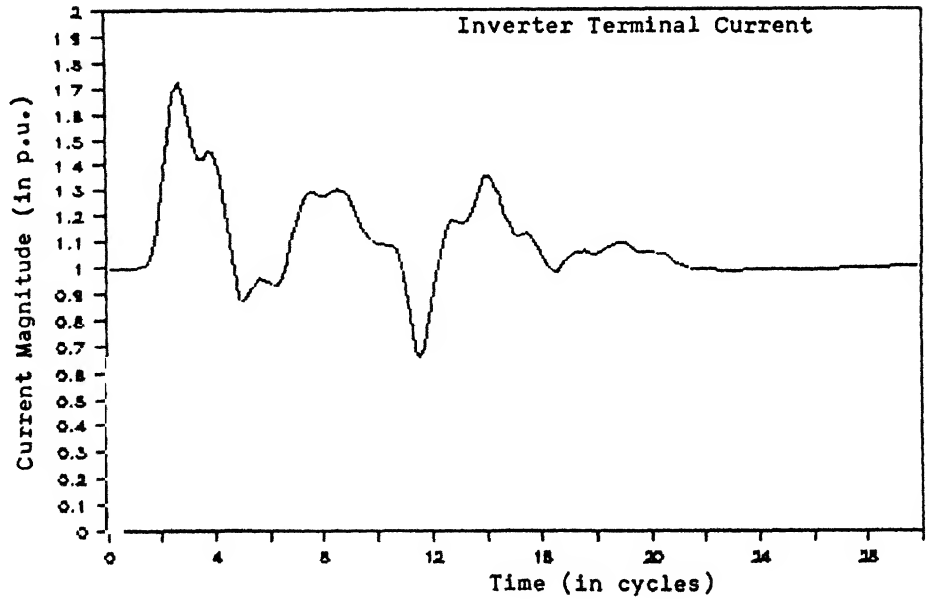




Fig. 3.17 20%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH MODIFICATION IN THE PROPOSED SCHEME



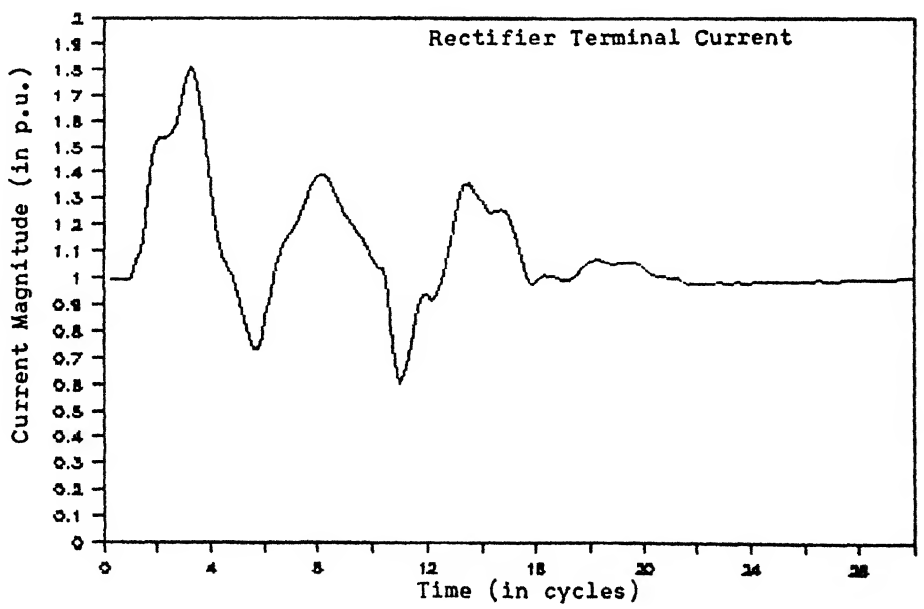
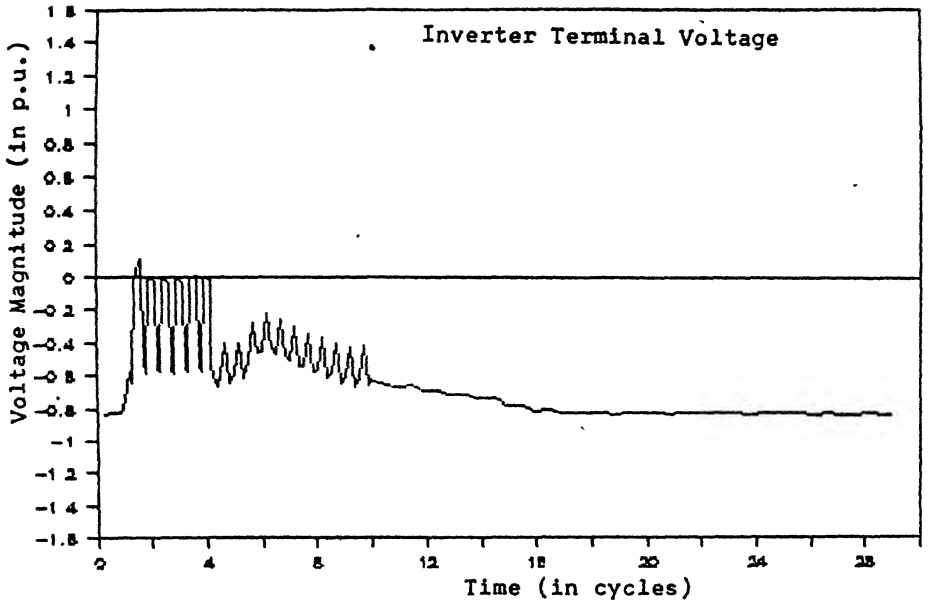
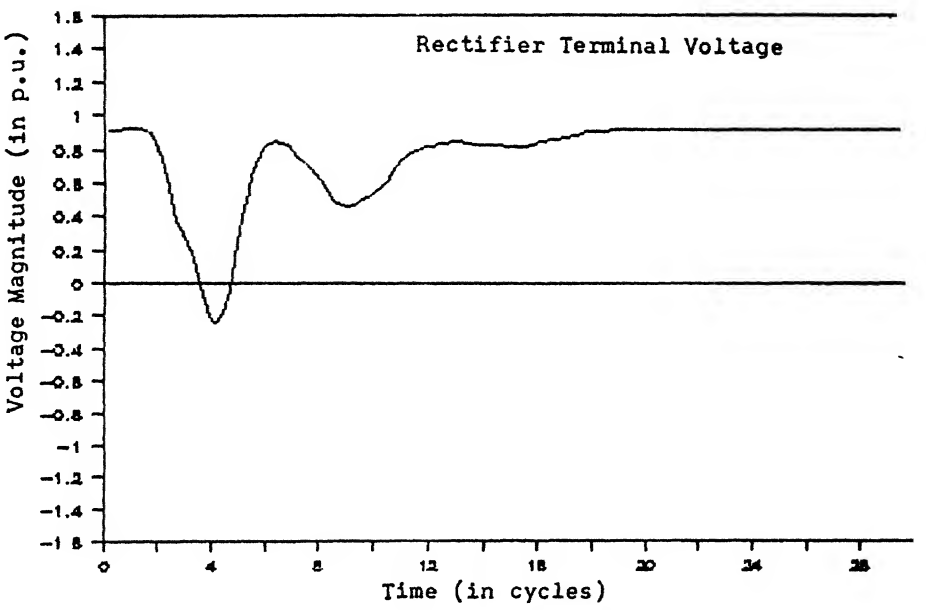
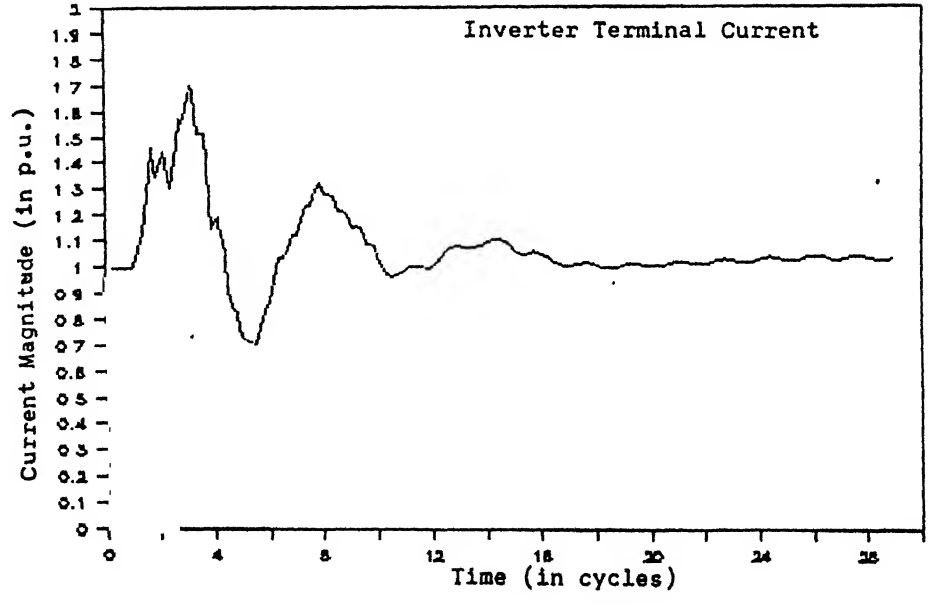




Fig. 3.18 50%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY



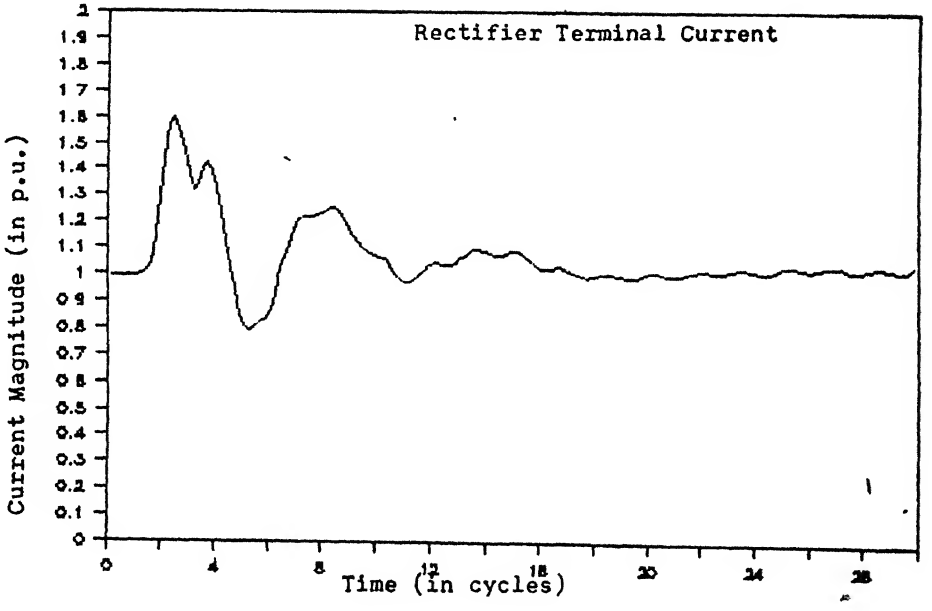
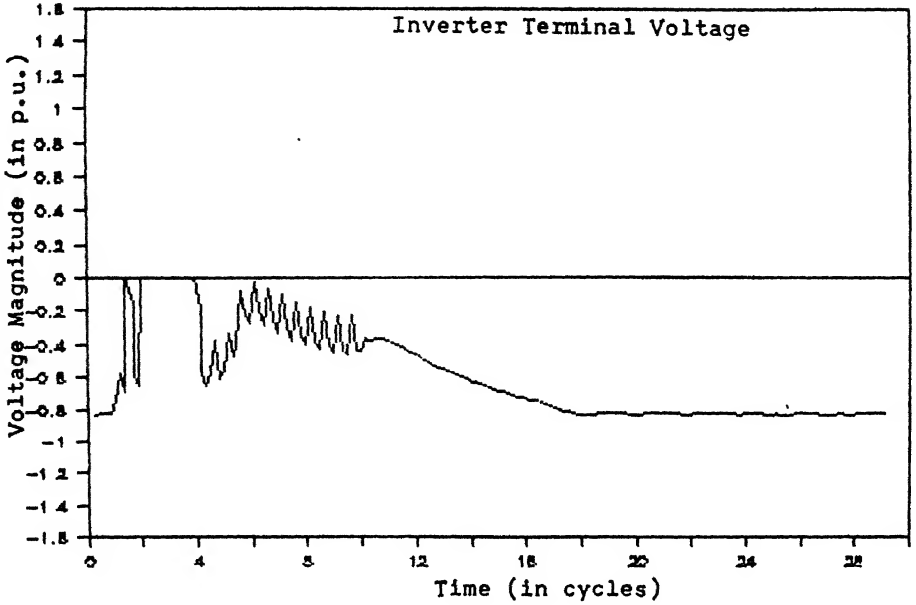
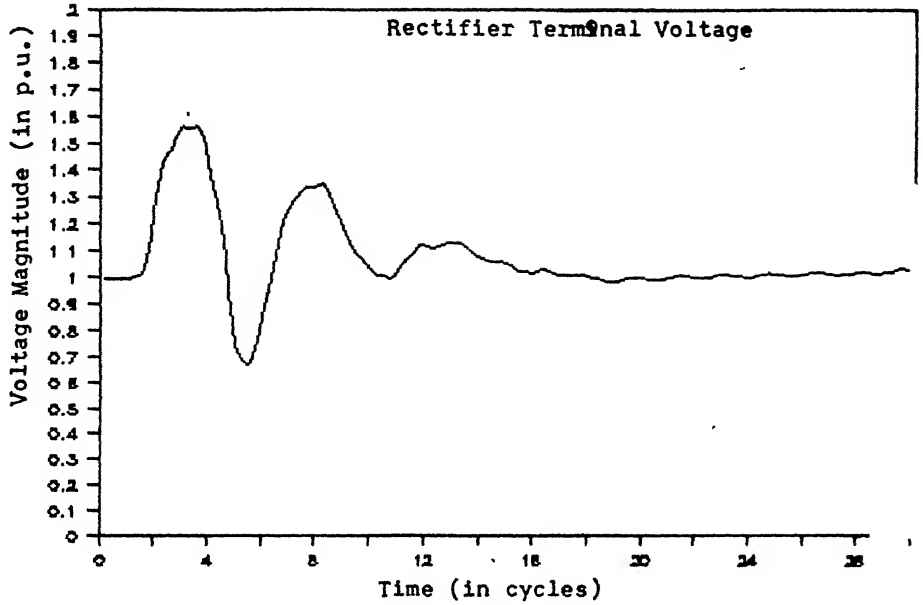
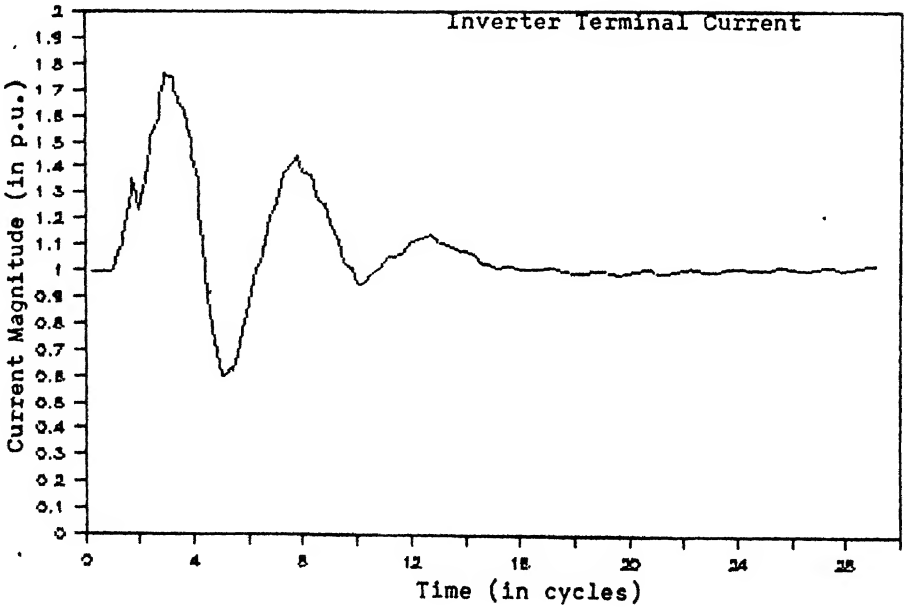




Fig. 3.19 50%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



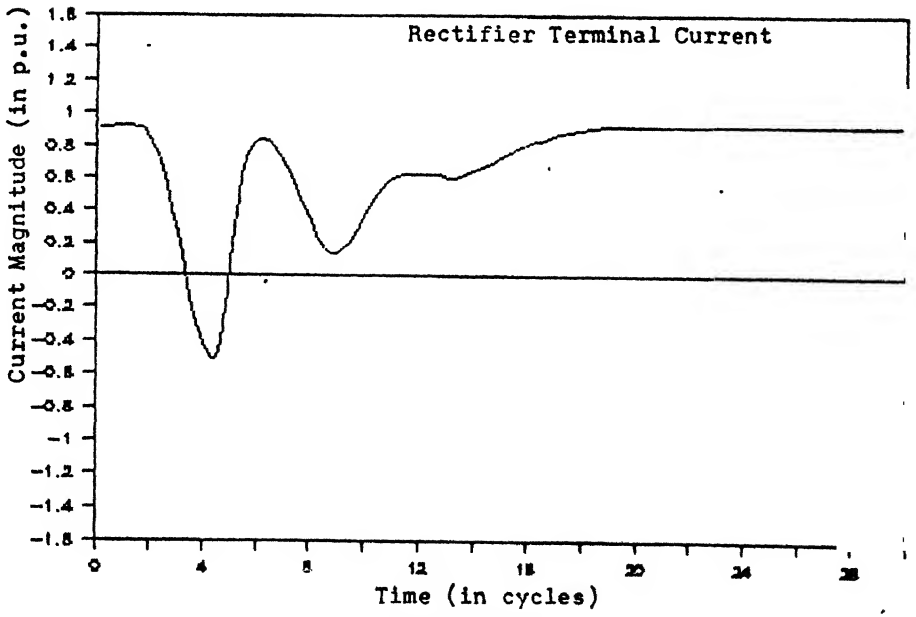




Fig. 3.20 50%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH MODIFICATION IN THE PROPOSED SCHEME

of the dip. This recovery procedure reduces the magnitude of oscillations in the line current and the rectifier terminal voltage. For a single phase to ground fault at the inverter terminal for 10 cycles, the system response is reported in Figs. 3.21 to 3.23. For this case, as can be observed from these figures, it is evident that the proposed recovery scheme does not improve the response to a great extent as it does in the previous cases except for the removal of the short circuit across the inverter terminal. This loads to additional oscillations in the current waveform and rectifier terminal voltage but does not hamper the process of recovery. This plots of inverter firing angle with the proposed recovery scheme has been produced in Fig. 3.24 and Fig. 3.25.

### 3.4.3 3-Phase to Ground Fault

In this section following cases are considered :

(a) 10 cycle 50% dip in all the three phases

(b) 4 cycle 99% dip in all the three phases.

The system response for these faults have been reported in Figs. 3.26 to 3.29. In all of these cases the advantage of the proposed recovery scheme is lost because with the symmetrical faults, there is no change in the zero-crossing of the commutation voltages which is an important consideration in advancing the firing. Moreover, the absence of the commutation voltages, as in the case of 3-phase to ground faults at

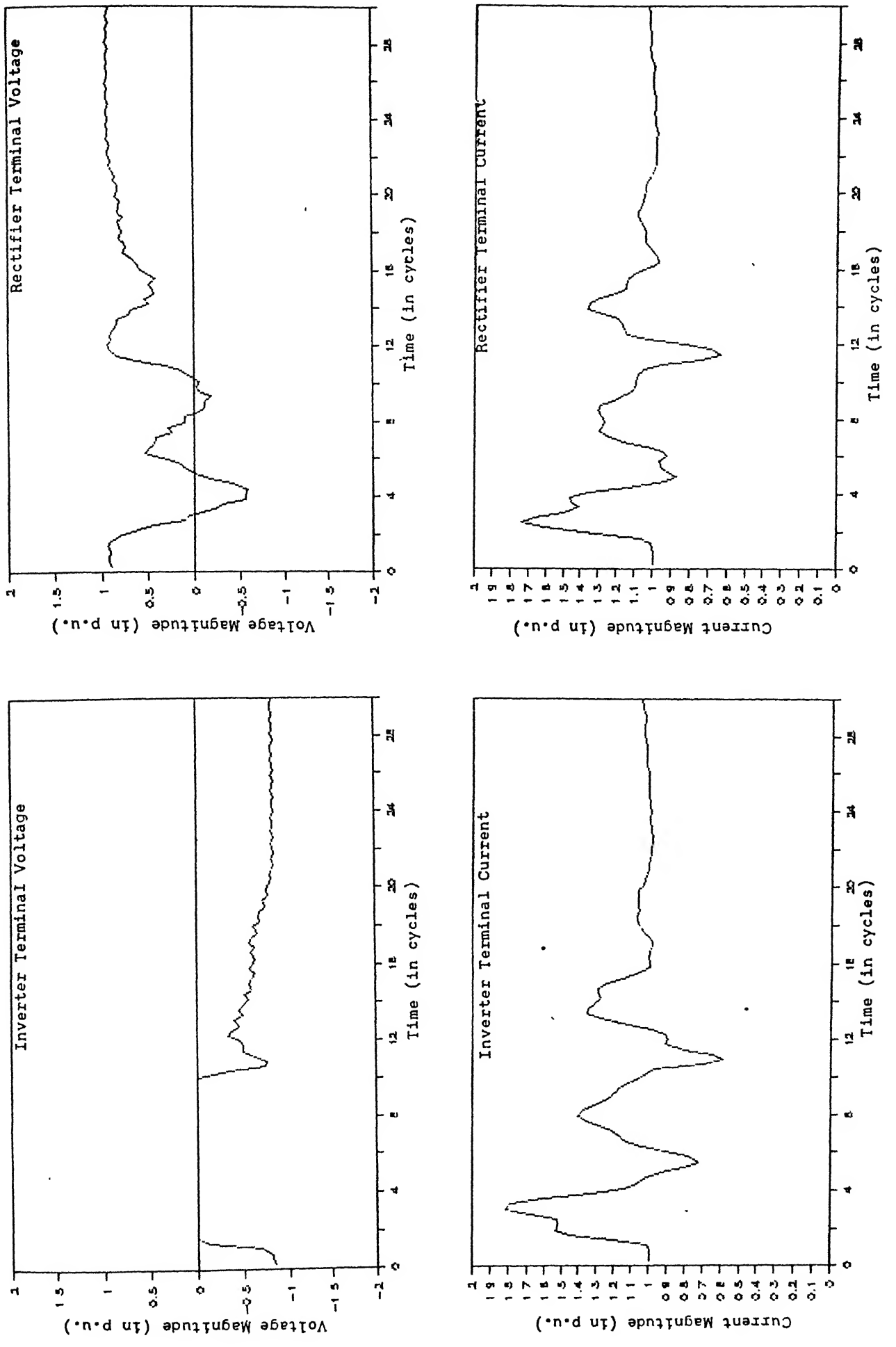
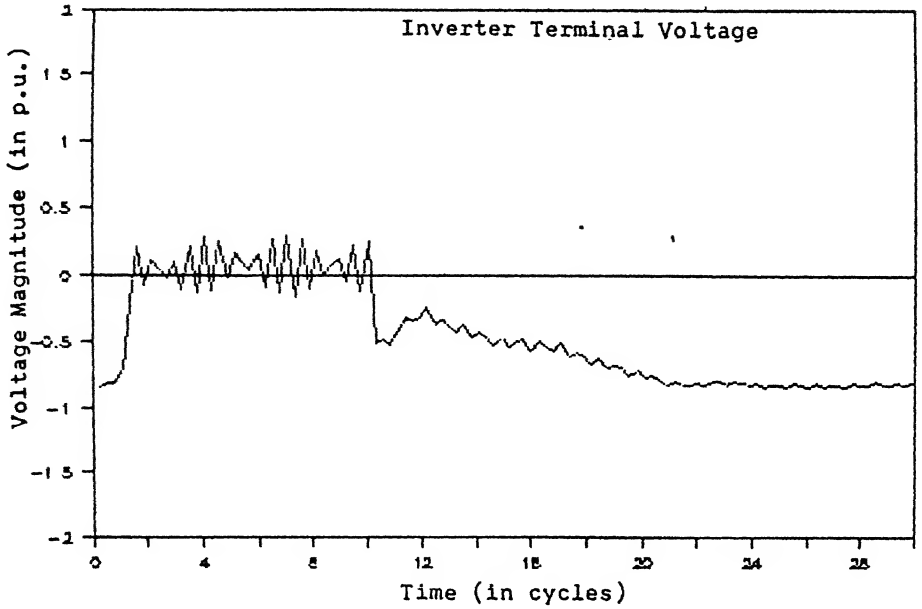
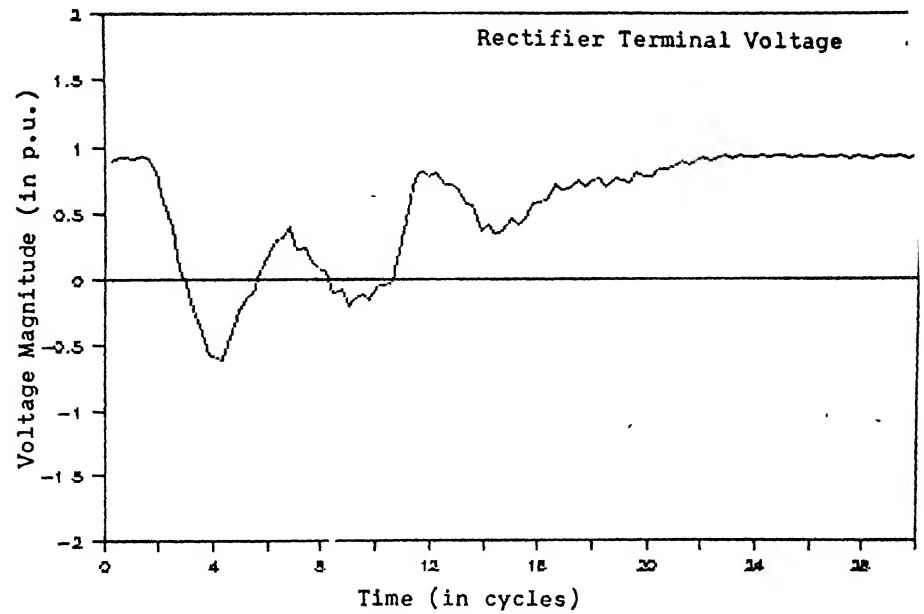
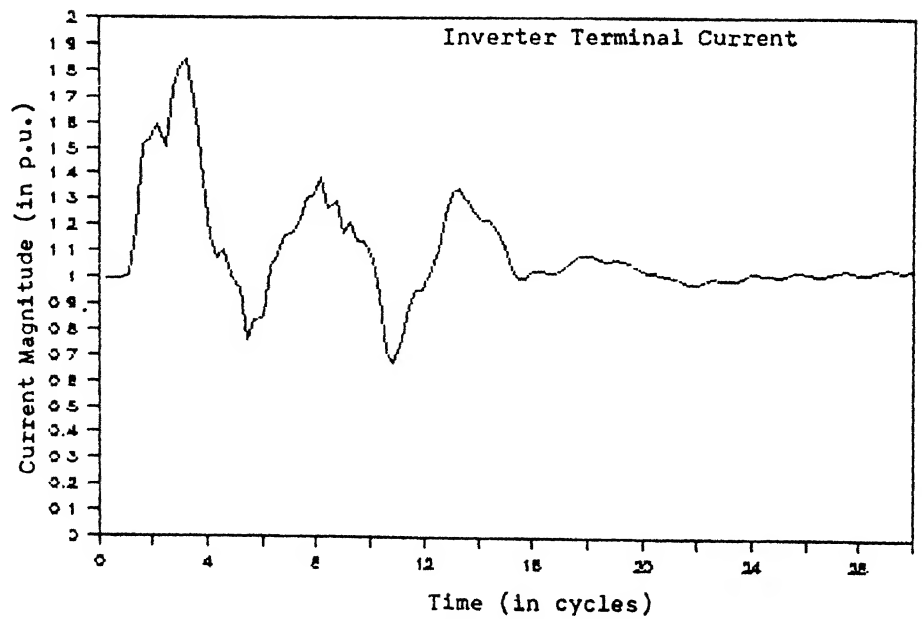



Fig. 3.21 99%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY



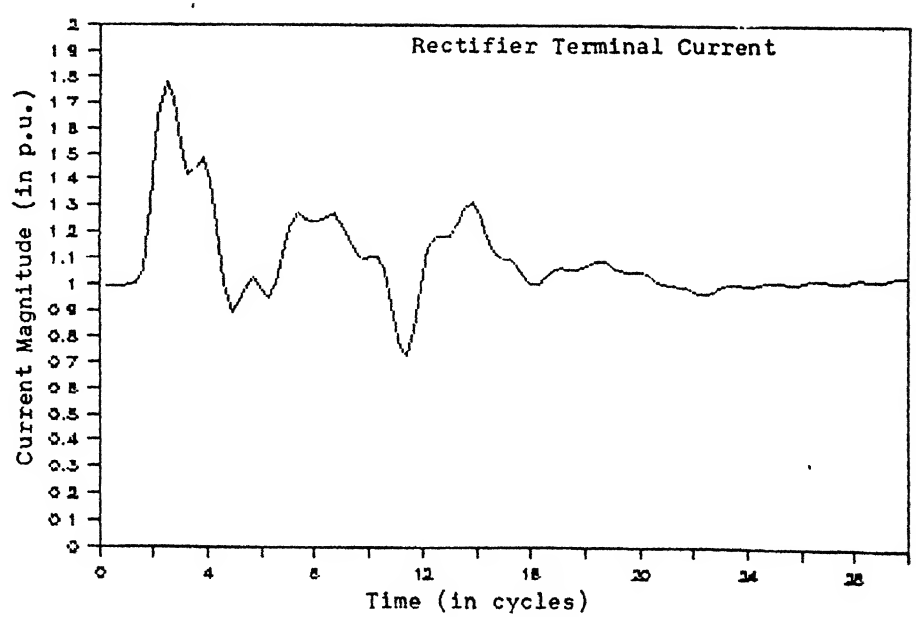
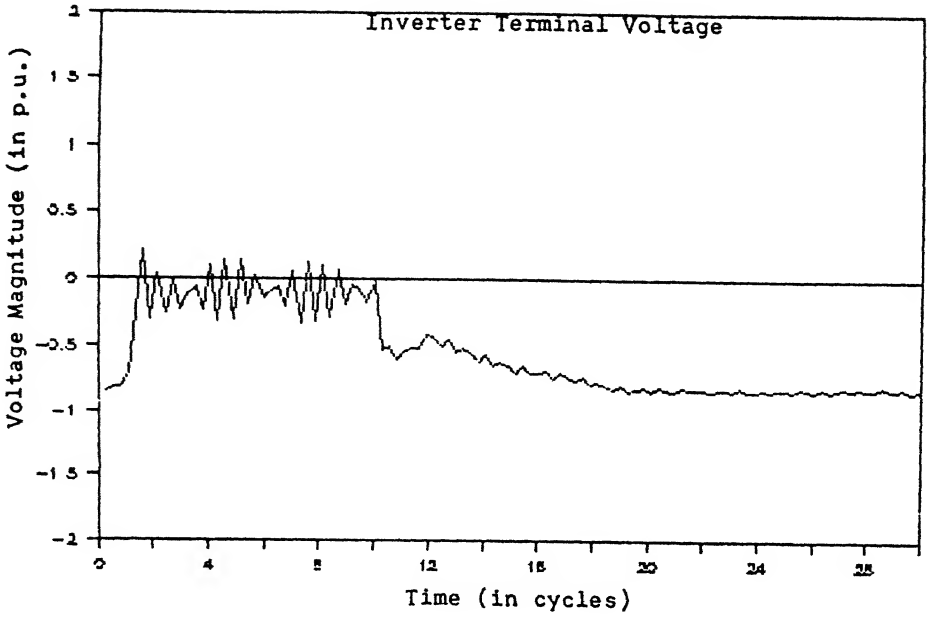
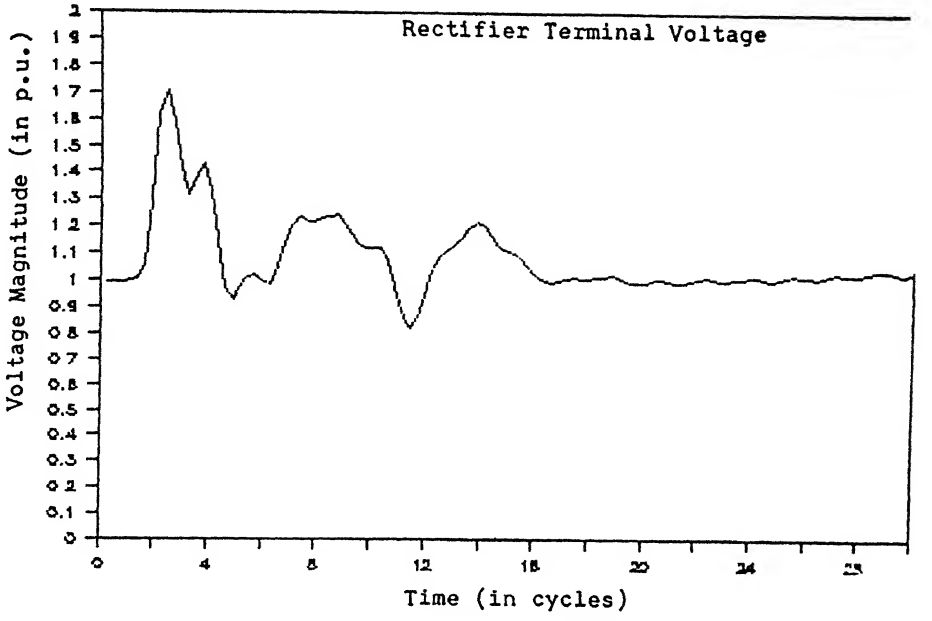
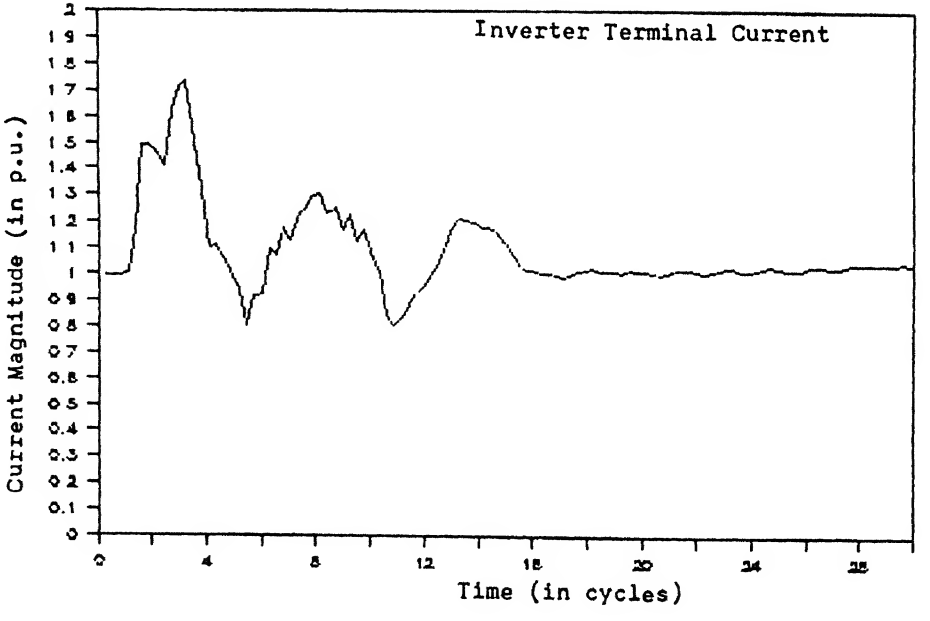




Fig. 3.22 99%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



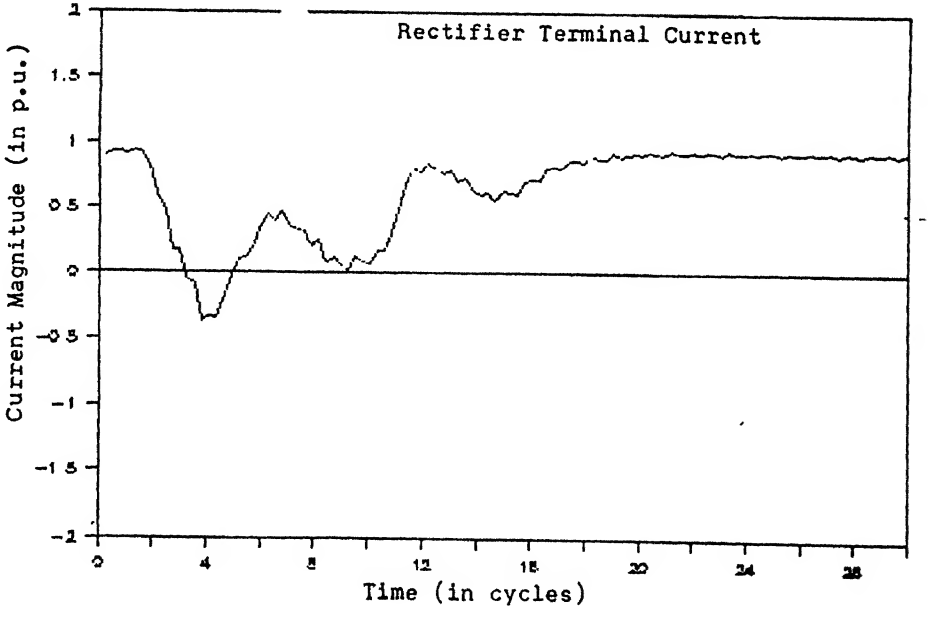
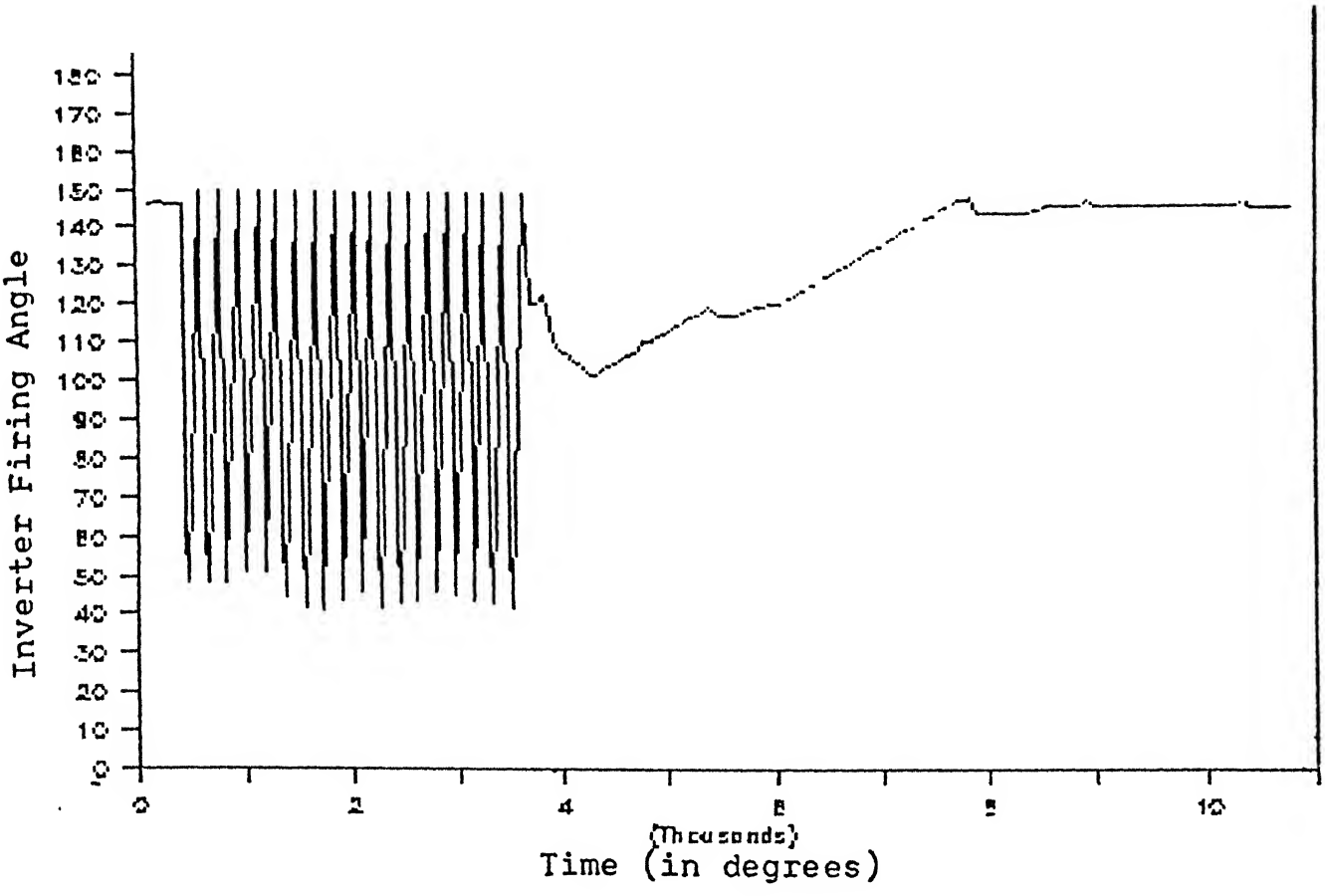




Fig. 3.23 99%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER WITH MODIFICATION IN THE PROPOSED SCHEME



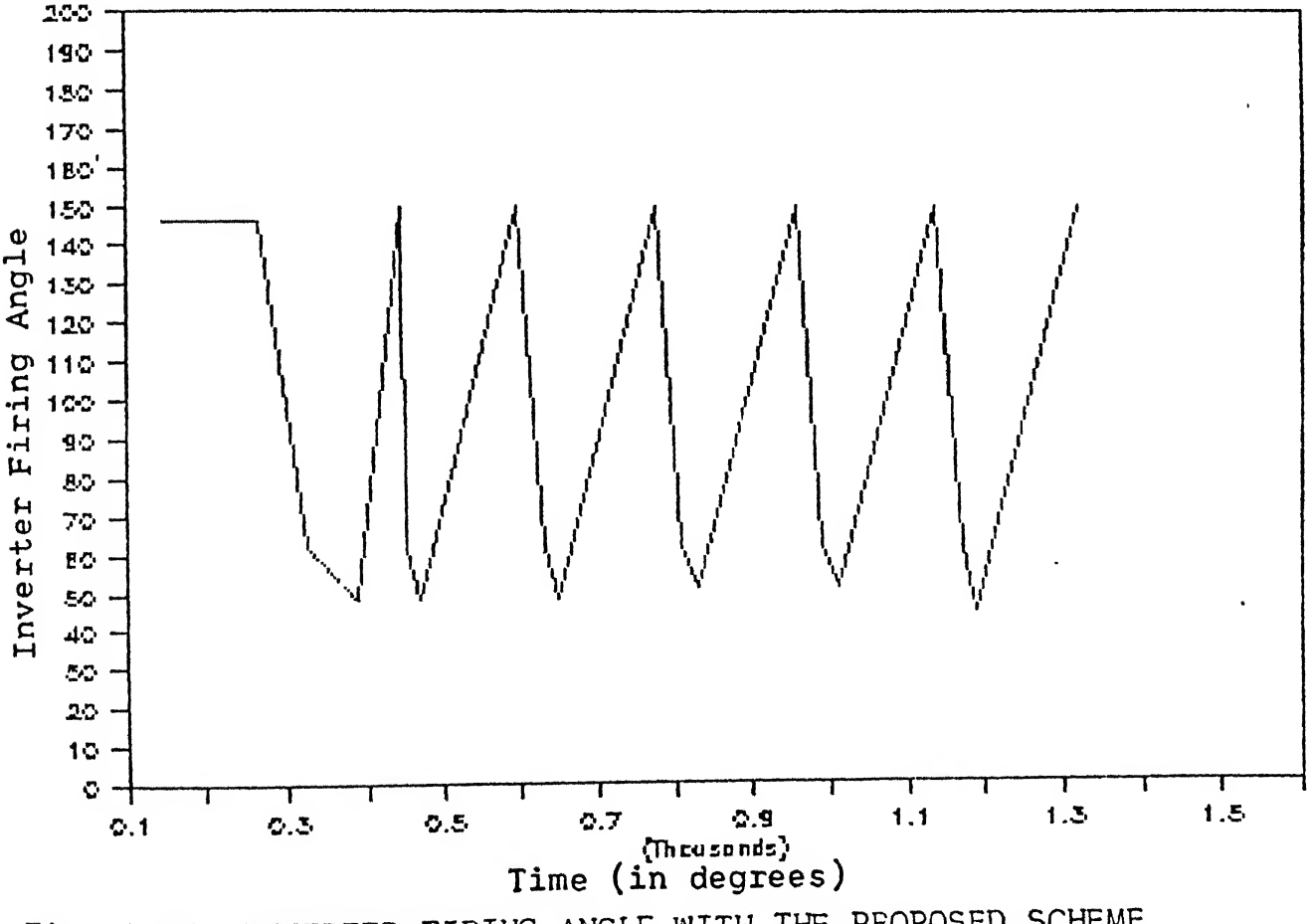




Fig. 3.24 INVERTER FIRING ANGLE WITH THE PROPOSED SCHEME

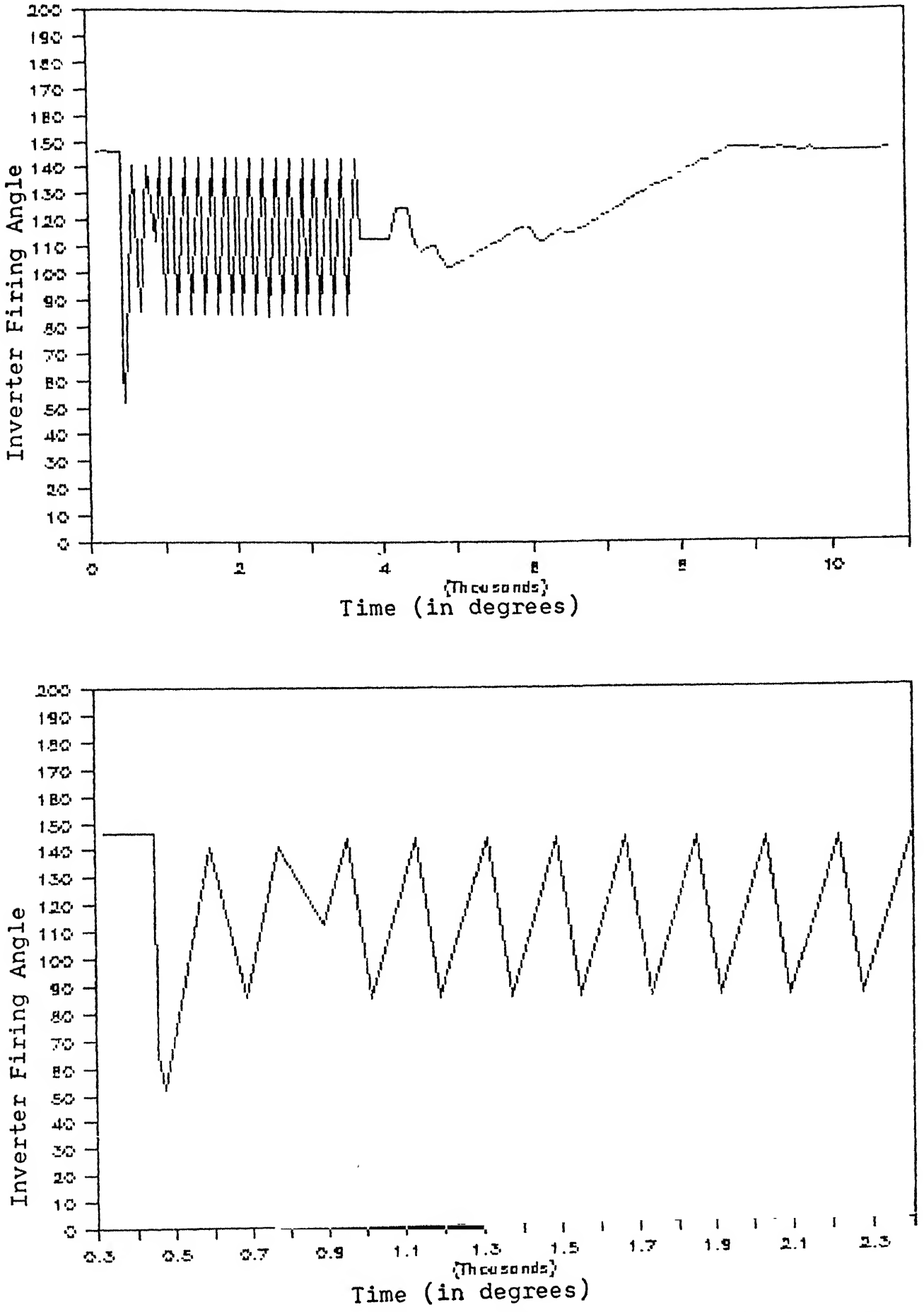
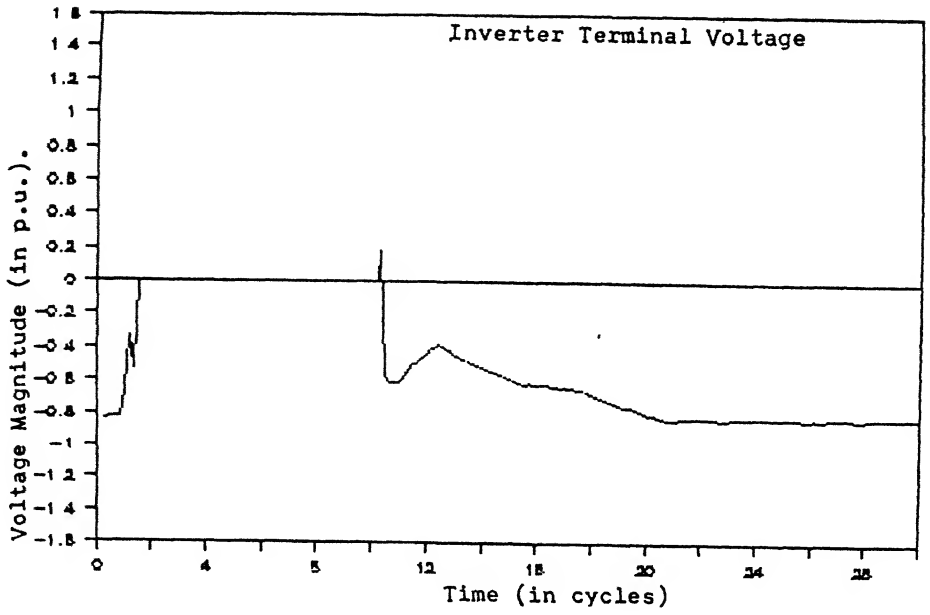
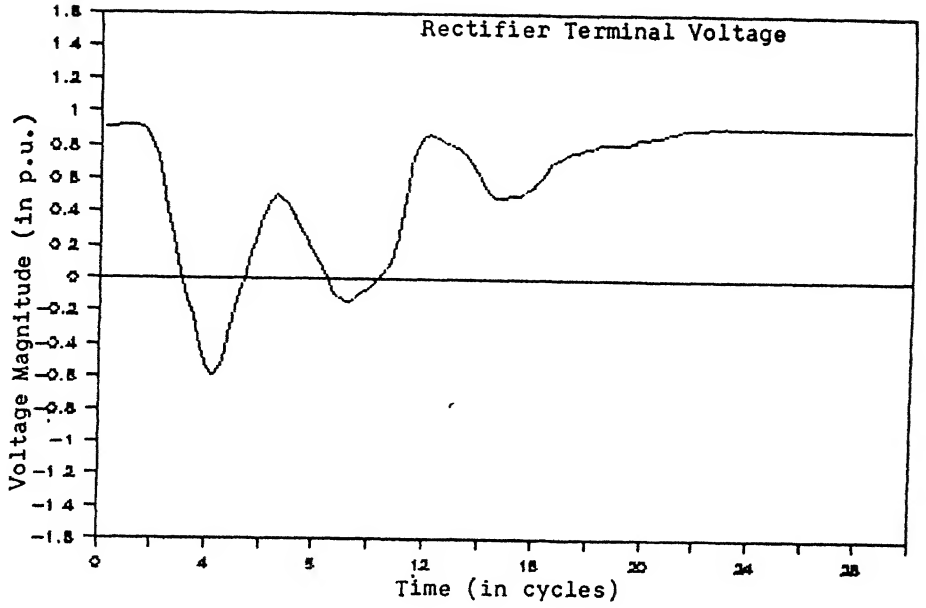
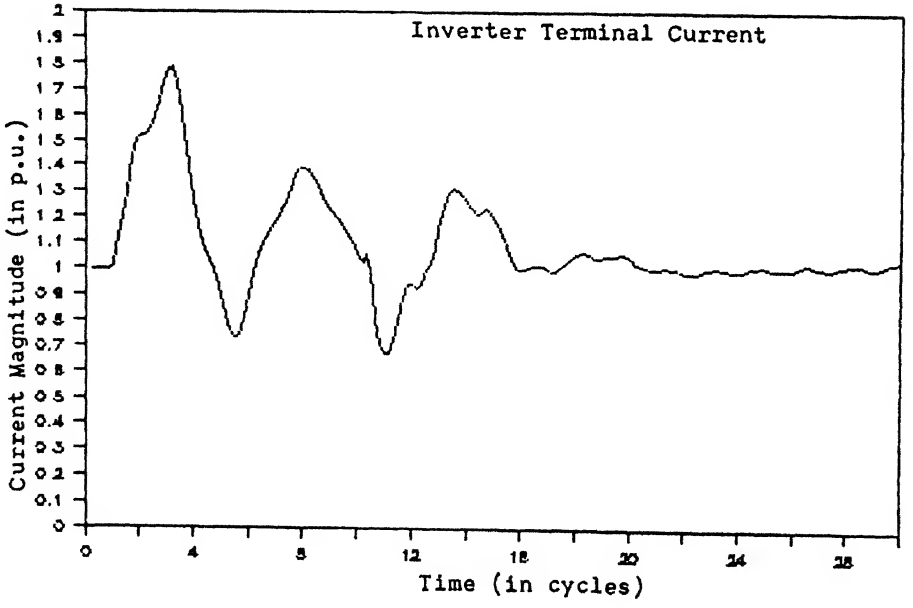



Fig. 3.25 INVERTER FIRING ANGLE WITH MODIFICATION IN THE PROPOSED SCHEME



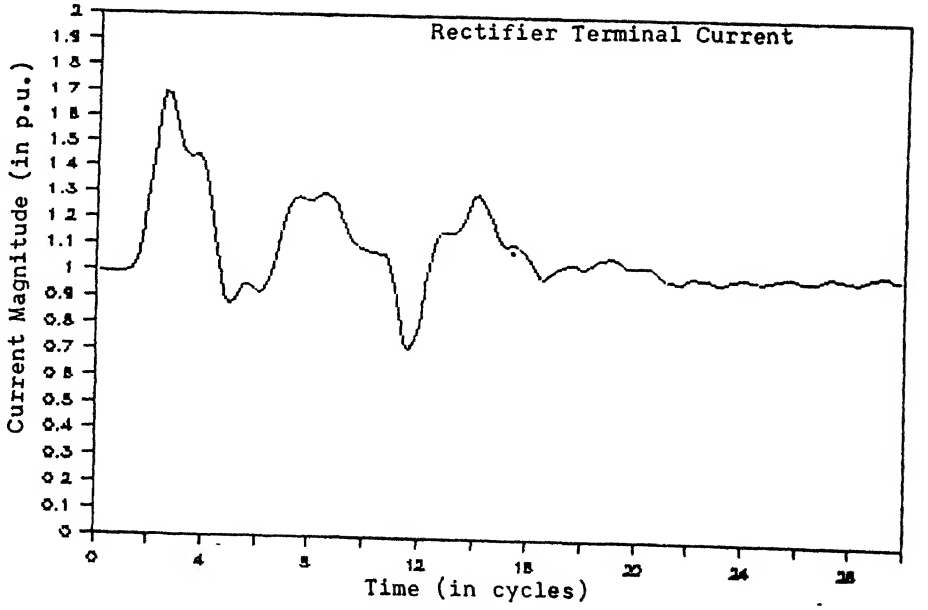
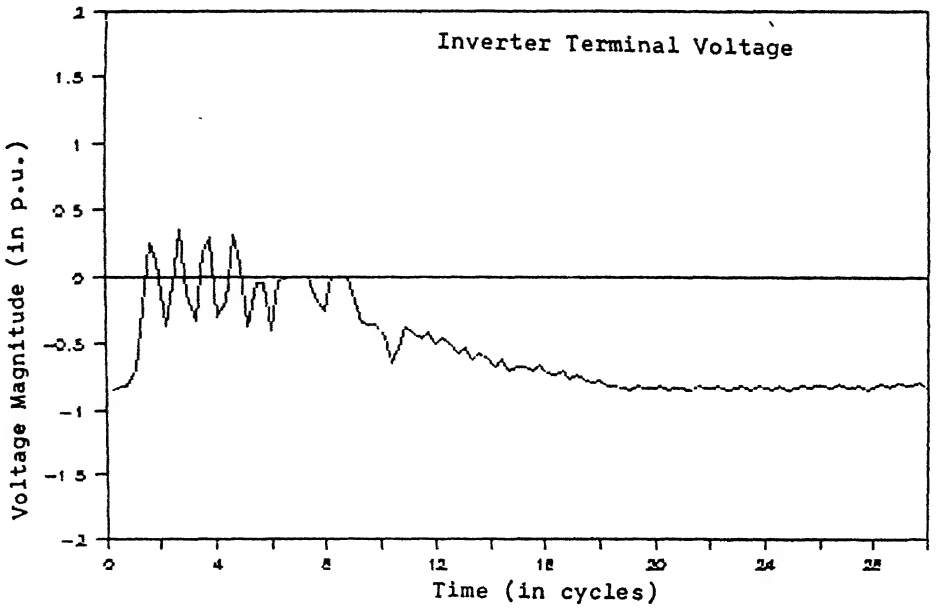
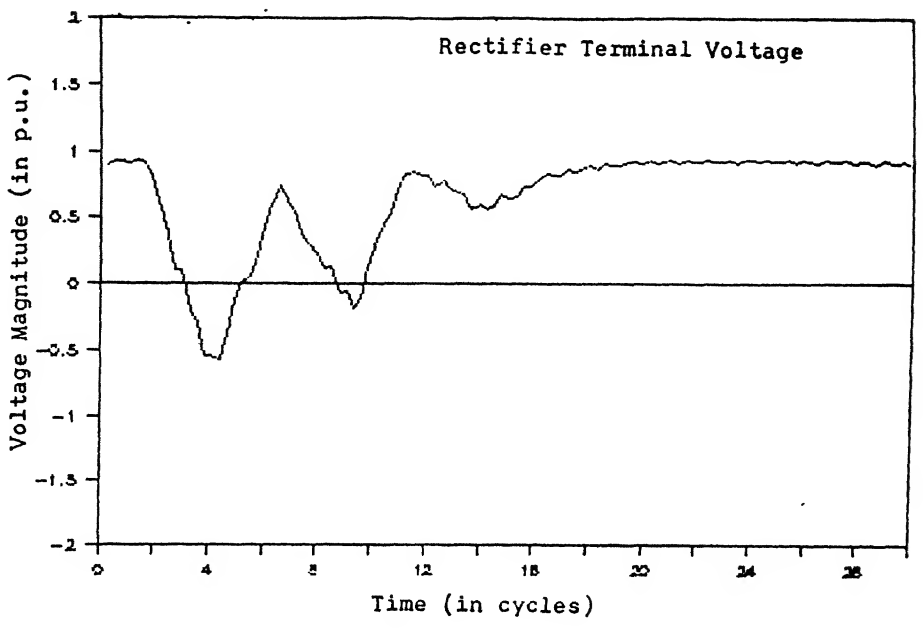
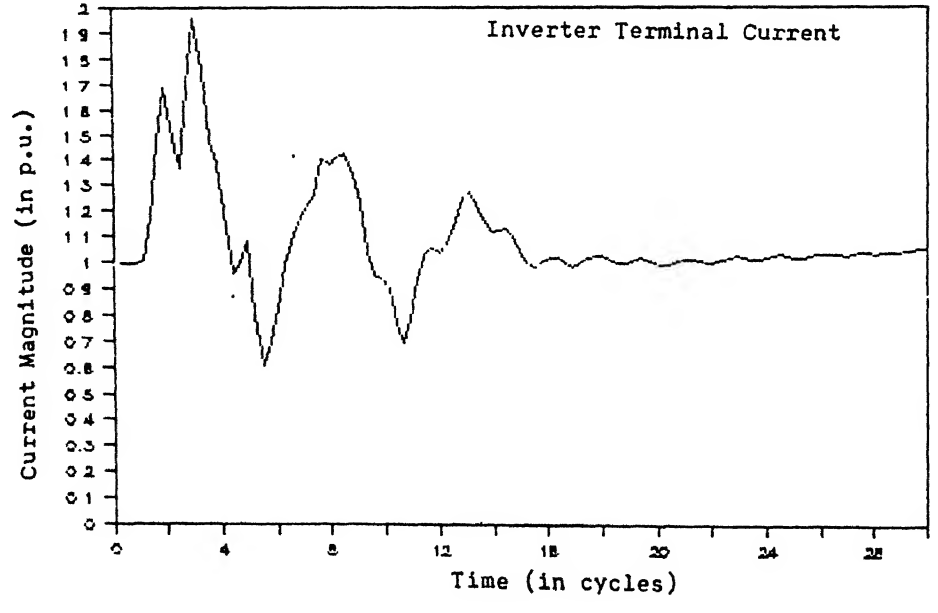




Fig. 3.26 50%, THREE PHASE, 10 CYCLE DIP AT INVERTER
NORMAL RECOVERY



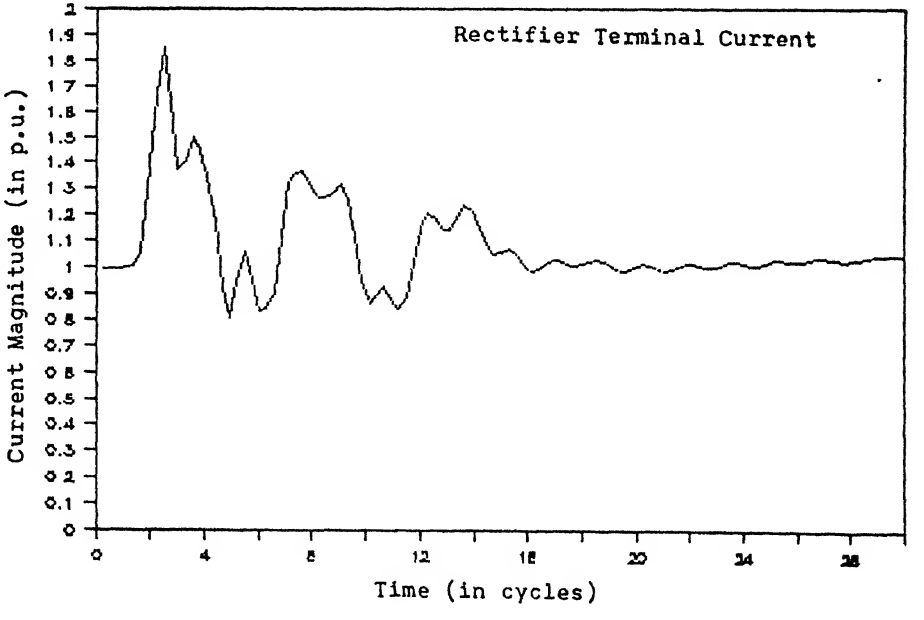
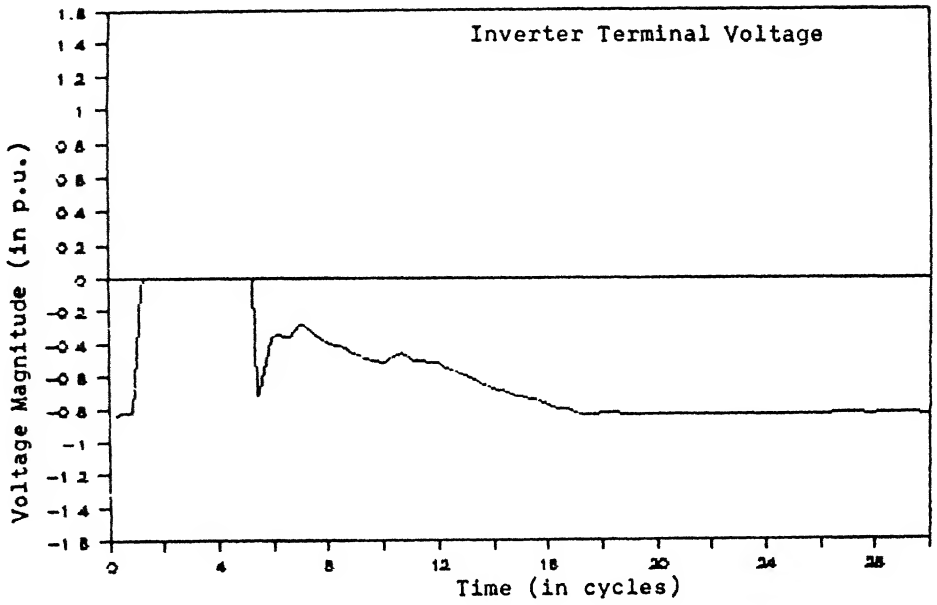
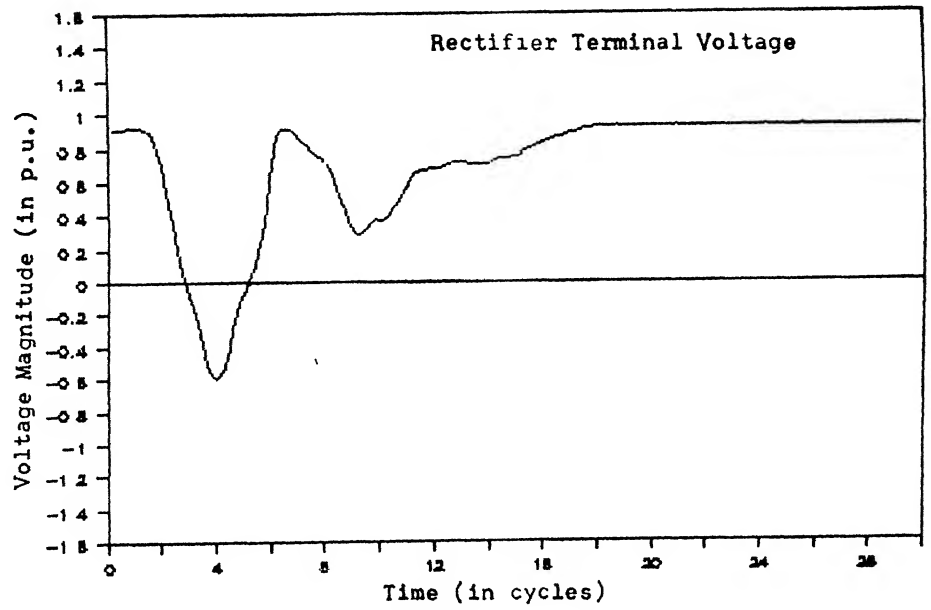
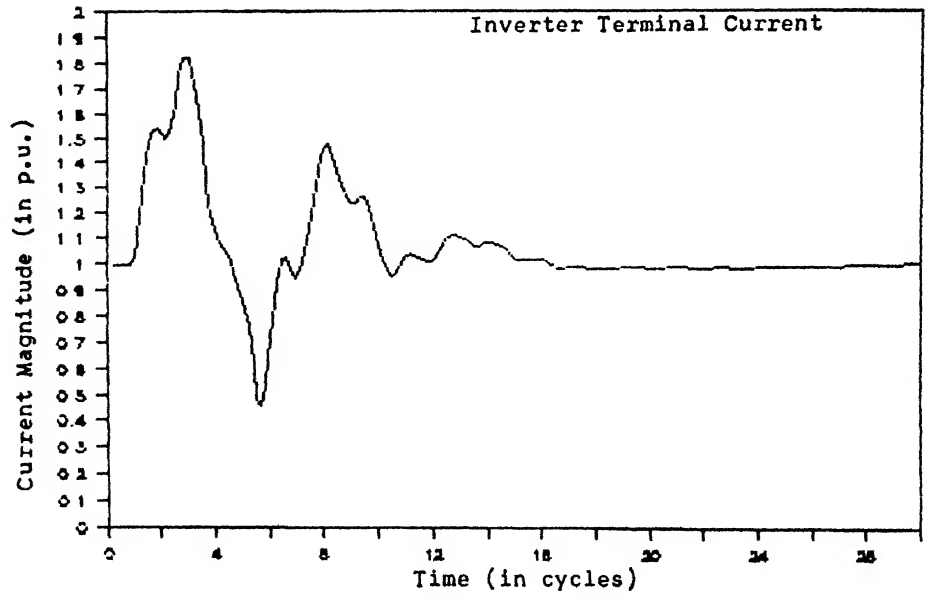




Fig. 3.27 50%, THREE PHASE, 10 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



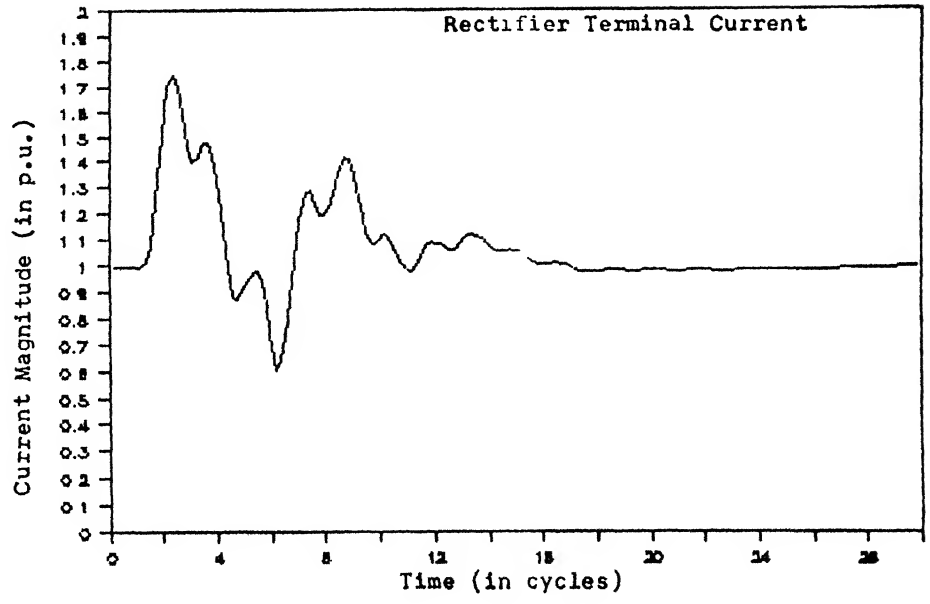
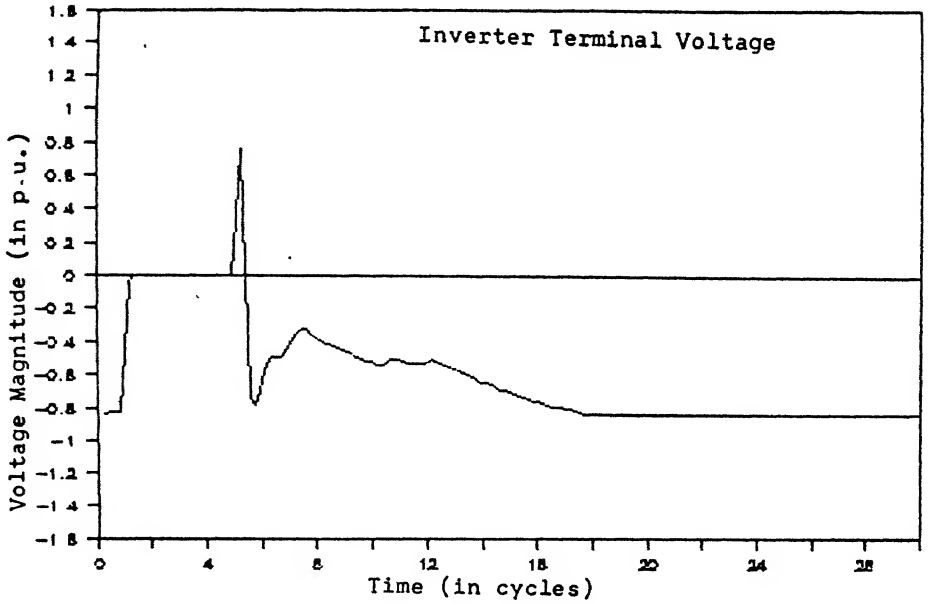
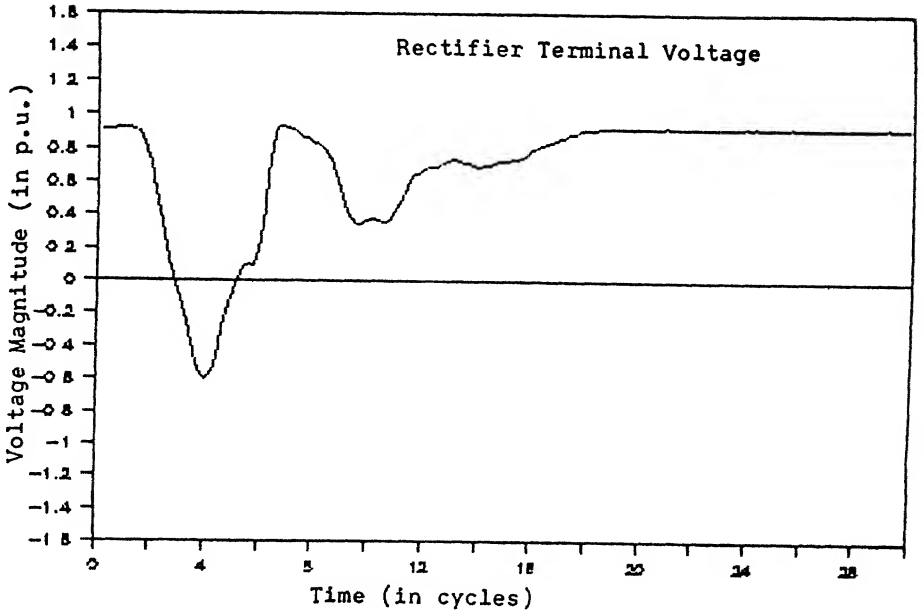
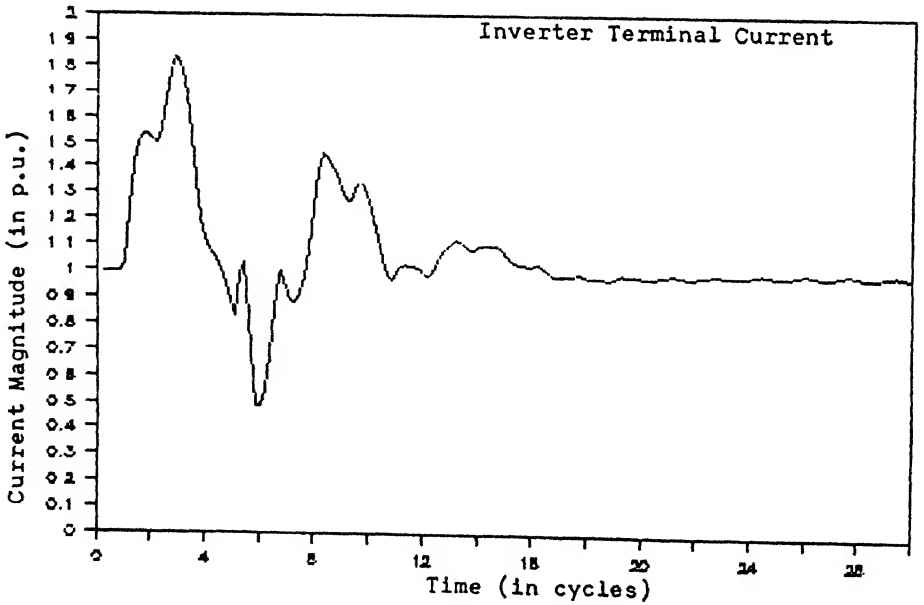




Fig. 3.28 99%, THREE PHASE, 4 CYCLE DIP AT INVERTER
NORMAL RECOVERY



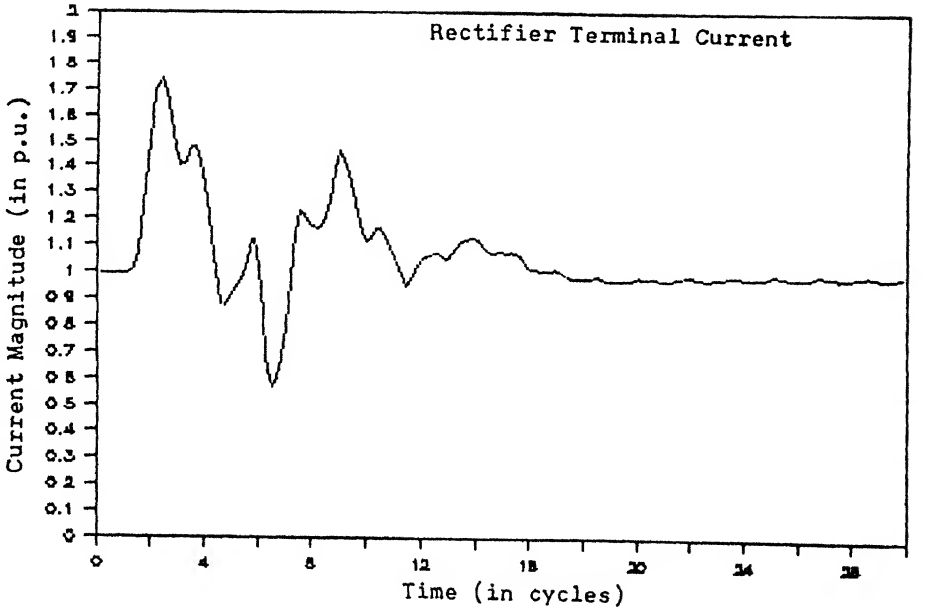




Fig. 3.29 99%, THREE PHASE, 4 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME

the inverter terminal, will prevent the firing of any valve. However, it can be noticed that the proposed recovery scheme does not lead to any adverse effect.

## 3.5 CONCLUSIONS

This chapter has been devoted to explore the possibility of a recovery scheme proposed to improve the system recovery following a commutation failure. Theoretical aspects of the proposed scheme have been explained. Various cases considering different types of faults have been studied for comparative evaluation of the proposed recovery scheme and the normal recovery process. Based on the various cases studied it can be concluded that proposed recovery scheme improves the system response to a great extent in case of remote and momentary faults but in case of prolonged severe and symmetrical faults the improvement is not much. However, it does not lead to any adverse effects.

# CHAPTER 4

## CASE STUDY OF NATIONAL HVDC EXPERIMENTAL PROJECT

### 4.1 INTRODUCTION

In order to further examine the effectiveness of the recovery scheme proposed in the previous chapter, a case study of the system for National HVDC (NHVDC) Experimental Project has been undertaken. The investigations are carried out based on digital simulation wherein the various components of NHVDC system are represented in detail.

### 4.2 NATIONAL HVDC PROJECT

National HVDC project was initiated in 1982. This is an experimental DC transmission line linking Andhra Pradesh State Electricity Board at Lower Sileru and Madhya Pradesh State Electricity Board at Barsoor. The project is expected to develop in 3 phases. Phase 1 of the project will be capable of transmitting 100 MW at +100 kV DC, 6 pulse Monopolar system with ground return. In Phase II of the project, it is planned to raise the capability of the system to transmit 200 MW of power at +200 kV DC, 12 pulse Monopole with ground return and in Phase III to 450 MW, at $\pm$ 200 kV DC, 12 pulse, Bipole. One of the 196 km long, 220 kV AC double circuit transmission line linking Lower Sileru and Barsoor is being planned to be used

to transfer 100 MW on direct voltage of 100 kV in Phase I. The power transmission will be monopolar in the initial stage and the ground electrode has been designed for continuous operation at 1000 A. 6-pulse converters used have double valve construction. Each valve consists of 96 thyristors in series. The thyristors are of 55 mm dia and 3.2 kV peak inverse voltage. The double valves are cooled by a close loop fine water system. The converter transformers are 40.5 MVA, 220/86.6 kV, single phase two winding. The on load tap changer control will have tap range from 22.5% to -10% in the steps of 1.25%. A 6th harmonic tuned and a high pass filter have been provided at each station. A smoothing reactor 0.45 H, 1000 A designed for 200 kV has been provided at each end of the line. One of the most important feature of the project is ground electrode system. Both the converter stations have ground electrode system for full power operation continuously, about 10 kms away from the stations.

## 4.3 SYSTEM REPRESENTATION

A HVDC system comprises of (1) AC system feeding the converters (2) converters with their associated controls and (3) DC network consisting of transmission lines and filter. An adequate representation of these components is required in the digital simulation of HVDC system. These component models are interfaced using appropriate interfacing variables.

In the National HVDC experimental project the AC system is considered to be quite strong, hence its representation is ignored in the present investigation. Rest of the constituents of the HVDC system are briefly described below.

### 4.3.1 Converter Representation

Each terminal of the NHVDC system consists of a single six pulse converter unit. The six pulse converter is modelled as a variable voltage source behind a variable impedance. Reference [7] describes the development of an equivalent circuit for a six pulse converter. This is based on the graph theoretic approach which enables to formulate the converter equations for all possible modes of operation assuming continuous DC link current.Convèrter equations are derived using cutset matrix and the basic circuit equations. The equivalent circuit of the six pulse converter is reproduced in Fig. 4.1. The voltage source ($e_{eq}$) in the equivalent circuit is a function of the converter AC bus voltage, and hence has to be computed at each time instant. The equivalent circuit parameters ($R_{eq}$, $L_{eq}$) are dependent on the converter conduction pattern and are recalculated every time the conduction pattern changes due to start or cessation of any valve. The source $V_s$ is included to represent the effect of the DC system, $R_d$, $L_d$ denote the resistance and inductance of the smoothing reactor.

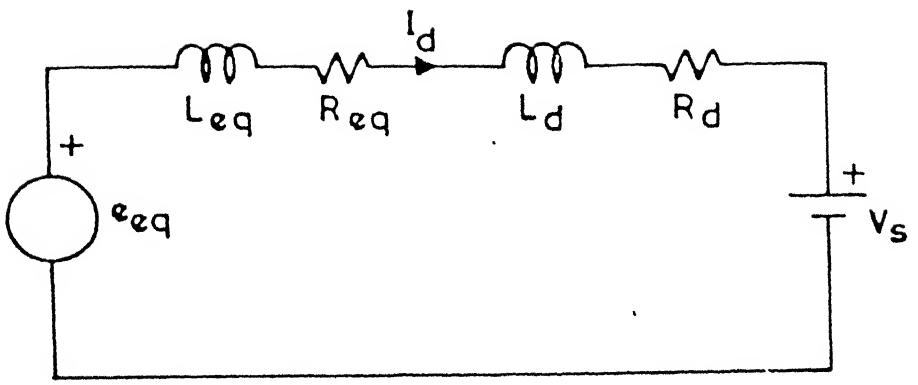



FIG. 4.1 EQUIVALENT CIRCUIT OF 6 PULSE CONVERTER

### 4.3.2 DC System Representation

The DC system comprises of the transmission line and the DC filters.

The transmission line is modelled as a $\pi$ equivalent circuit with the shunt arms consisting of capacitors and the series arm having a combination of resistance and inductance. A state variable representation of the line is used choosing the capacitor voltages and inductor currents as state variables. A more practical representation of the line would call for a number of $\pi$ sections as shown in Fig. 4.2. However, a single $\pi$ section representation is used in simulating the NHVDC system.

Filters are provided on the DC transmission line to eliminate the 6th and 12th harmonics from the DC current. The filter configuration and its representation in the state variable form is given in Appendix C.

### 4.3.3 Control Representation

Each converter in a HVDC system is equipped with a controller which determines the instant of firing of each valve. The performance of the HVDC line is critically dependent on the performance of its control system. Normally current control is used at the rectifier and constant extinction angle control at the inverter. In NHVDC system an equidistant pulse firing scheme (EPC) with pulse frequency control is used. At both the terminals, the interval between two successive firing

instants, called the interfiring period (IFP), is calculated as

$$IFP = 60^{o} + Q$$

where Q is the firing correction factor calculated by the respective controller. In steady state Q = 0 and firing takes place at every $60^{o}$ interval for a six pulse converter.

4.3.3.1 Current Controller

Figure 4.3 shows the block diagram for the current controller used in NHVDC system [ 9 ]. In this control system firing pulses are generated using voltage controlled oscillator, the frequency of which is determined by the firing correction factor (Q). A constant slope ramp function is generated starting from zero at each firing. This ramp function is compared to the sum of the firing correction factor Q and a bias equal to $60^{o}$, and a pulse is initiated at each instant of equality. The firing pulses at the output of the oscillator are separated for individual valves by a ring counter.

The firing correction factor (Q) is obtained as

$$Q = K_F (\alpha - \alpha_{act}) \quad \text{(Refer Fig. 4.3)}$$

where $\alpha$ is the control signal and $\alpha_{act}$ is the measured value of the preceding firing angle.

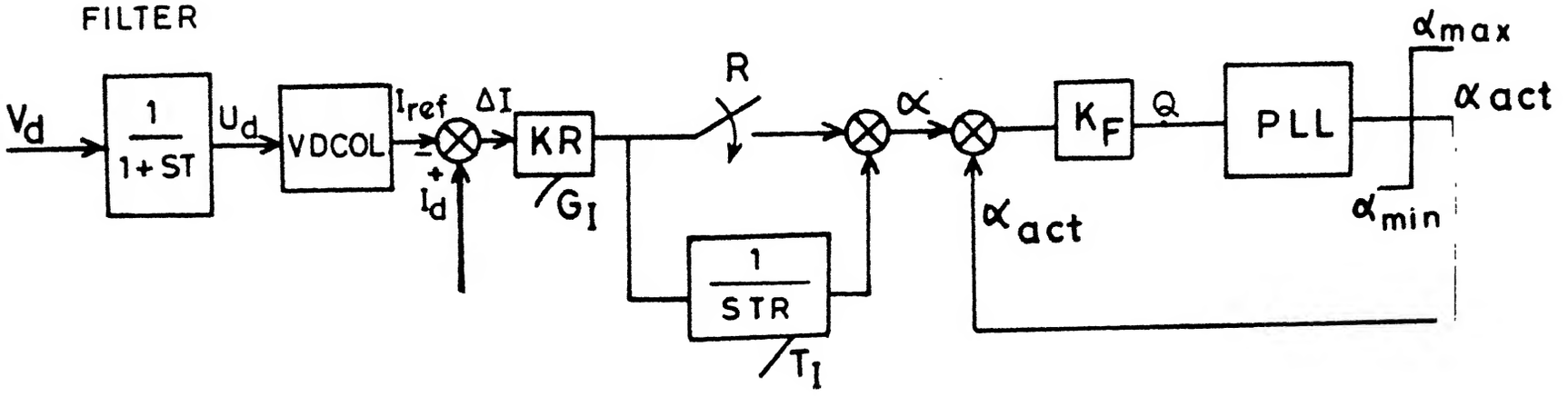



FIG. 4.3 BLOCK DIAGRAM OF THE CURRENT CONTROLLER .

The control signal is a function of the converter current and the reference current. The controller generating the control signal has a Proportional Integral (PI) characteristic in case of operating at rectifier and has a Integral characteristic in case of operating at inverter. For this, switch R is kept closed in case of rectifier and is left opened in case of inverter. Hence, the control signal ($\alpha$) in case of rectifier is

$$\alpha = K_R (I_d - I_{ref}) + \frac{K_R}{sT_R} (I_d - I_{ref})$$

and in case of inverter is

$$\alpha = \frac{G_I}{sT_I} (I_d - I_{ref})$$

where $I_d$ is the converter dc current

$I_{ref}$ is the reference current obtained from VDCOL characteristic

$K_R$ is rectifier gain

$G_I$ is inverter gain

$T_R$ is controller time constant at rectifier

$T_I$ is controller time constant at inverter

$s$ is d/dt

The values of the various parameters are given in Appendix B.

Voltage dependent current order limit (VDCOL) is implemented at both rectifier and inverter terminals. The function of VDCOL is to monitor the dc voltage of the converter obtained after the smoothing reactor and modify the current reference setting if the voltage goes below a fixed value in the event of a fault. The VDCOL characteristic used in NHVDC system is shown in Fig. 4.4 and details about its parameters are given in Appendix B.

4.3.3.2 Constant Extinction Angle Control (CEA)

Extinction angle ($\gamma$) is measured for each valve as the interval between the current zero instant of a particular valve and the instant at which the voltage across it becomes positive again. CEA controller attempts to keep this angle at its specified minimum value by changing the firing instant according to the difference between the measured and reference.

CEA control used in the present study is an equidistant pulse control [5]. The firing correction factor is obtained as

$$Q = K\ (\gamma - \gamma_{ref})$$

where

$\gamma$ is the measured value of preceding extinction angle

$\gamma_{ref}$ is the reference value of

K is the gain of the controller

Q is calculated only when the measured $\gamma$ is less than the reference $\gamma$. In case the measured $\gamma$ is greater than reference

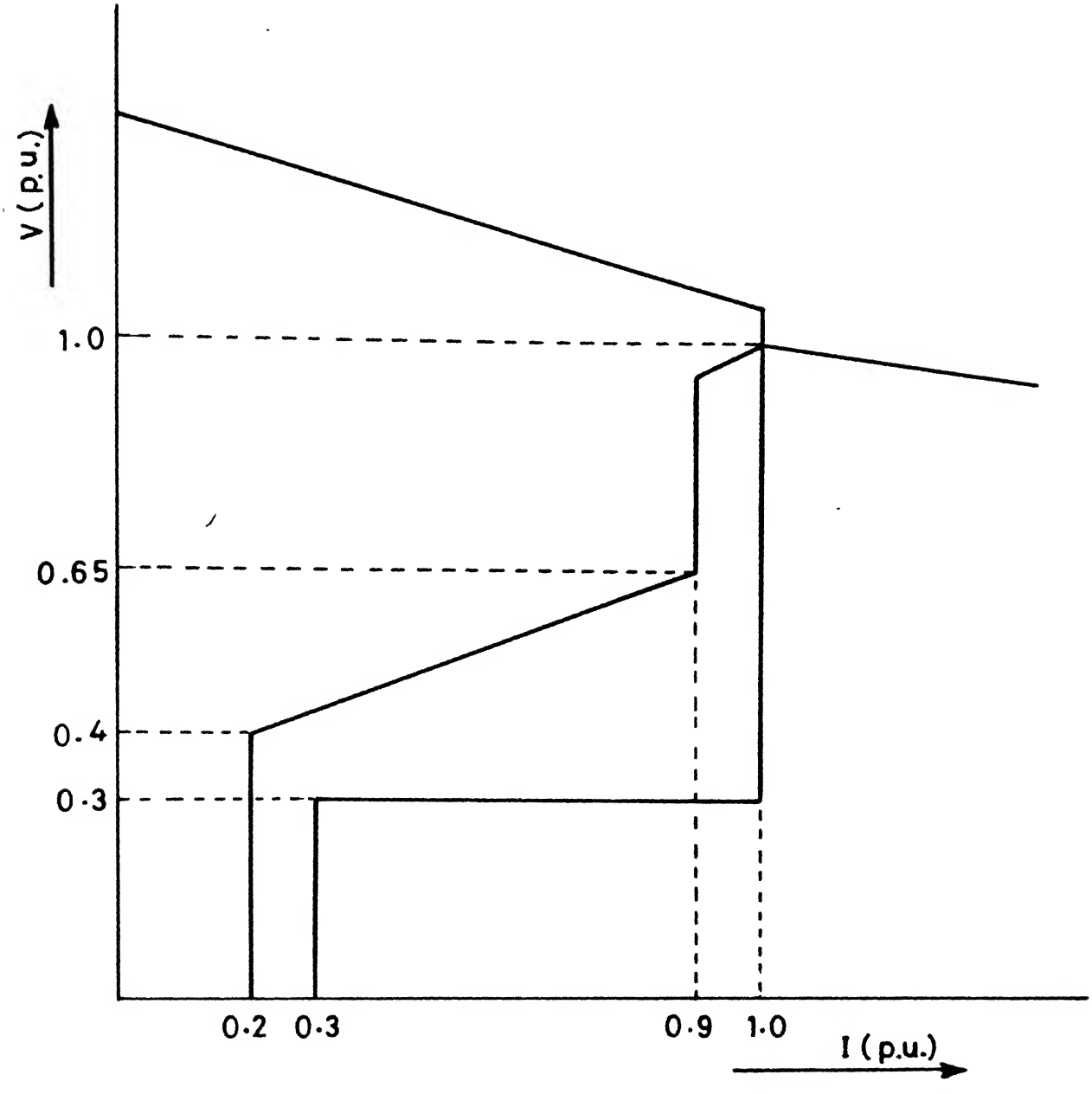



FIG. 4.4 VDCOL CHARACTERISTIC .

$\gamma$ , Q = O. Since inverter safety is of predominant concern, gain K is given a large value.

## 4.4 SIMULATION PROGRAM

The development of a Digital Computer program for simulating HVDC systems is described in [7]. This incorporates both 6 and 12 pulse converter representation along with analog firing control schemes based on Individual Phase Control (DPC) and Equidistant Pulse Control (EPC). The program has been modified to take into account various components of NHVDC system.

The simulation can start either assuming the system under steady state condition or zero initial conditions. In case of former, the initial condition for various state variables have to be supplied. Various state variable can be calculated with the help of various parameters given in Appendix B.

In the simulation program the minimum limit on firing angle ($\alpha_{min}$) at rectifier is incorporated by restricting the firing of any valve until the commutation voltage of that valve has reached a defined minimum positive value. In a similar manner maximum limit on firing angle ($\alpha$) is also imposed. Another salient feature of the program is the change over of the controls. When the inverter current falls below its reference value, the operation is changed to constant current control mode. To avoid changing the control mode for a momentary variation in current, the decision of changing the

mode of control is based on a measurement of current through a first order time delay element. If this measured current is below the reference current of the inverter current controller, the operation is switched over to constant current control from CEA control. The reverse transition of control occurs when the measured extinction angle for any valve is less than the reference value.

The program is suitably augmented to take into account the proposed recovery scheme.

## 4.5 CASE STUDY

For the comparative evaluation of the proposed scheme, following cases have been studied on the NHVDC system.

1) A short duration single phase to ground fault either at a remote location in the AC system or at the inverter AC bus.
2) A prolonged single phase to ground fault either at a remote location in the AC system or at the inverter AC bus.
3) A 3-phase to ground fault either at a remote location or at the inverter AC bus.

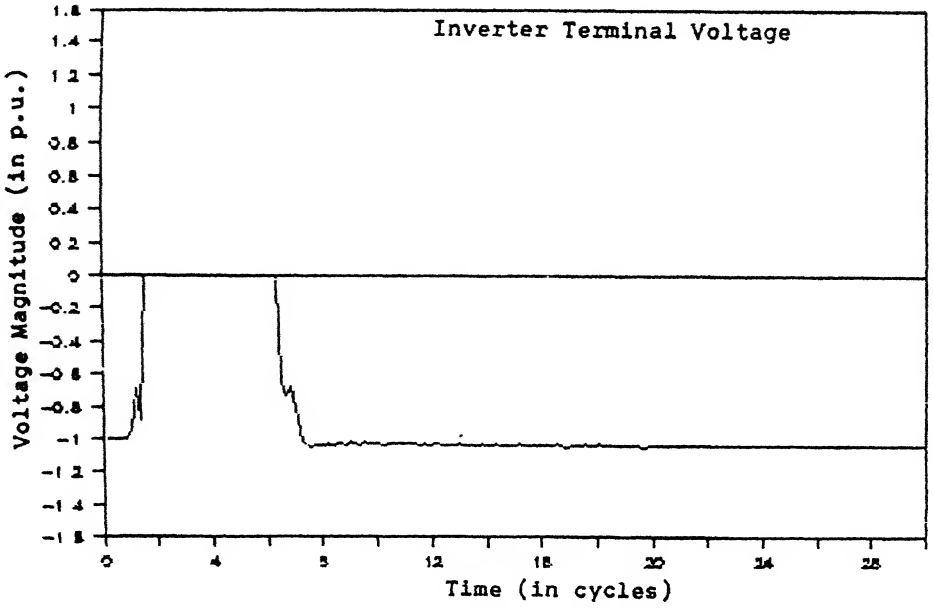
### 4.5.1 Short Duration Single Phase to Ground Faults

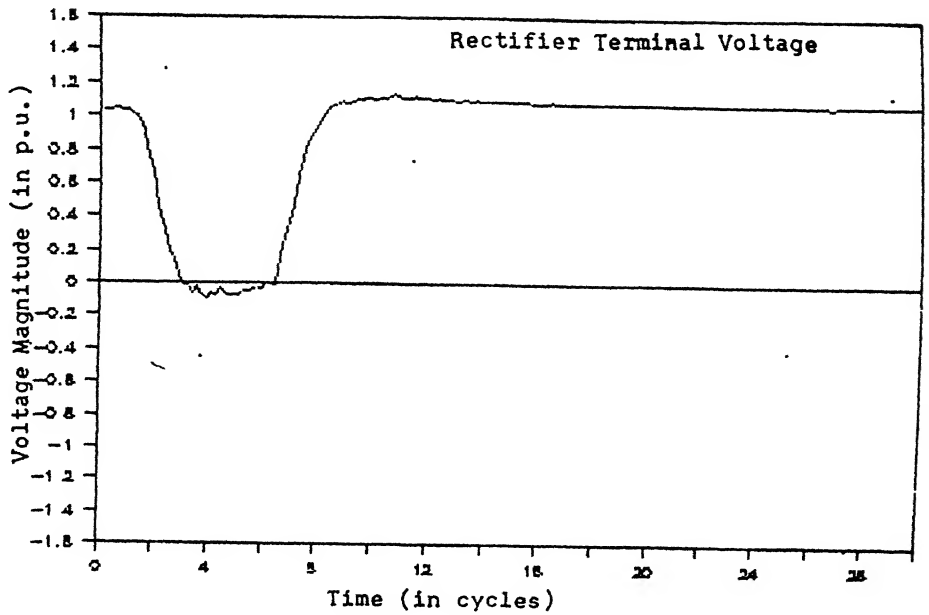
In this section following faults are considered :

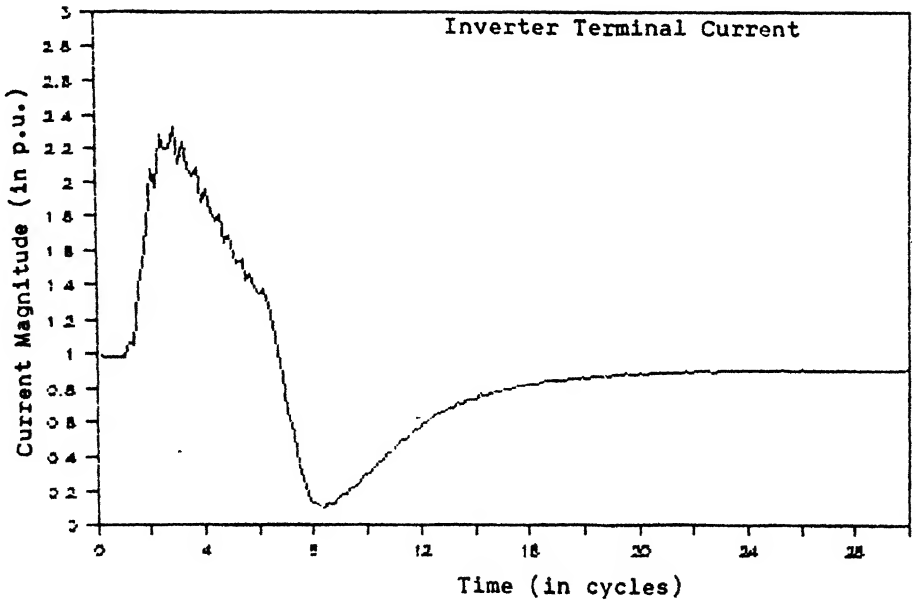
a) Single cycle, 50% dip in phase A voltage

b) Single cycle, 99% dip in phase A voltage

The response of the system following the fault in case A, are given in Figs. 4.5 and 4.6. Fig. 4.5 shows the system performance with normal recovery and Fig. 4.6 shows the same with the proposed recovery scheme. In the two figures 4.5 and 4.6, it can be noticed that for a momentary 50% dip in phase A voltage, the short circuit across the inverter terminal persists for a duration of about 6 cycles with the normal recovery process whereas with the proposed recovery scheme the duration of short circuit has been reduced drastically (about half a cycle). Because of this reduction in the duration of short circuit the oscillations in the line current have been reduced to a low peak value. With the normal recovery process, the rectifier terminal voltage also undergoes a considerable variation which has been reduced to a great extent with the proposed recovery scheme. Hence, it is evident that system response has improved considerably with the proposed recovery scheme. Figs. 4.7 and 4.8 show the system response following a fault of case B. Figs. 4.7 and 4.8 show the system response with normal recovery and with proposed recovery scheme respectively. It is evident from these figures that the proposed recovery scheme has improved the system response



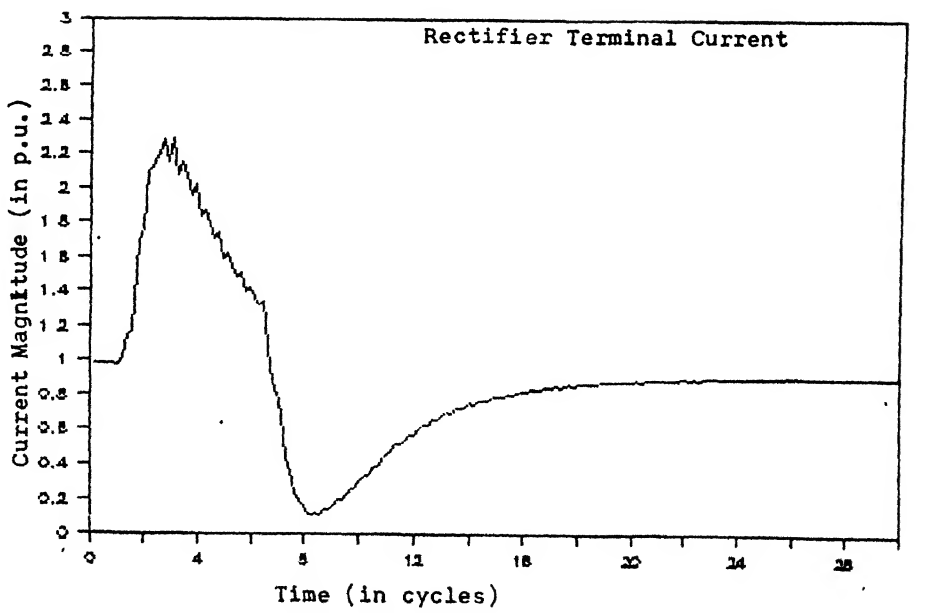
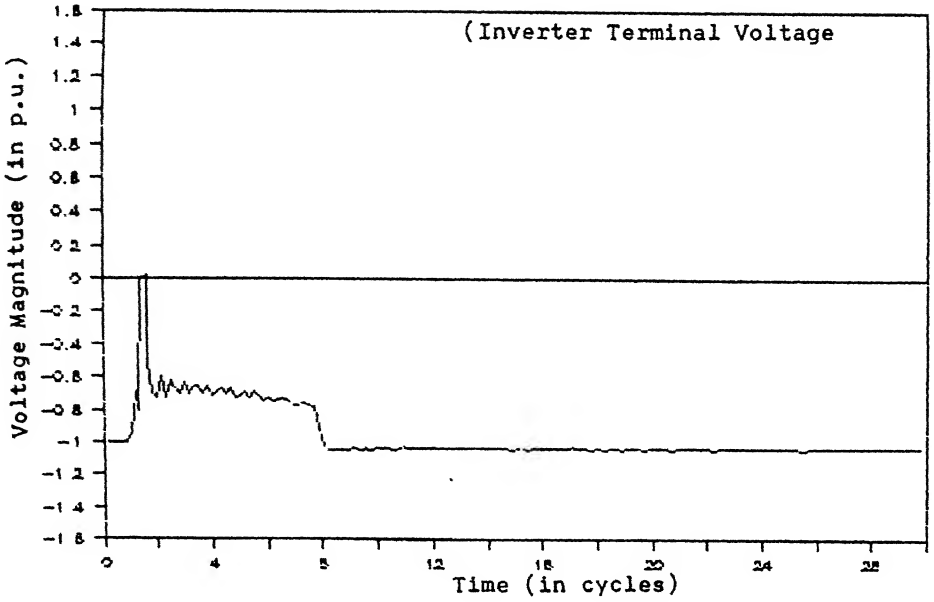
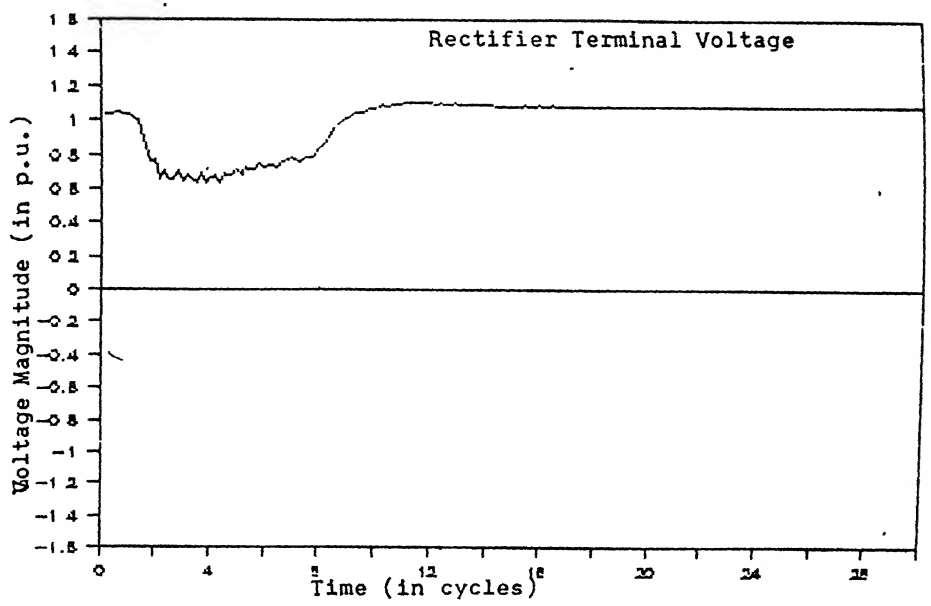
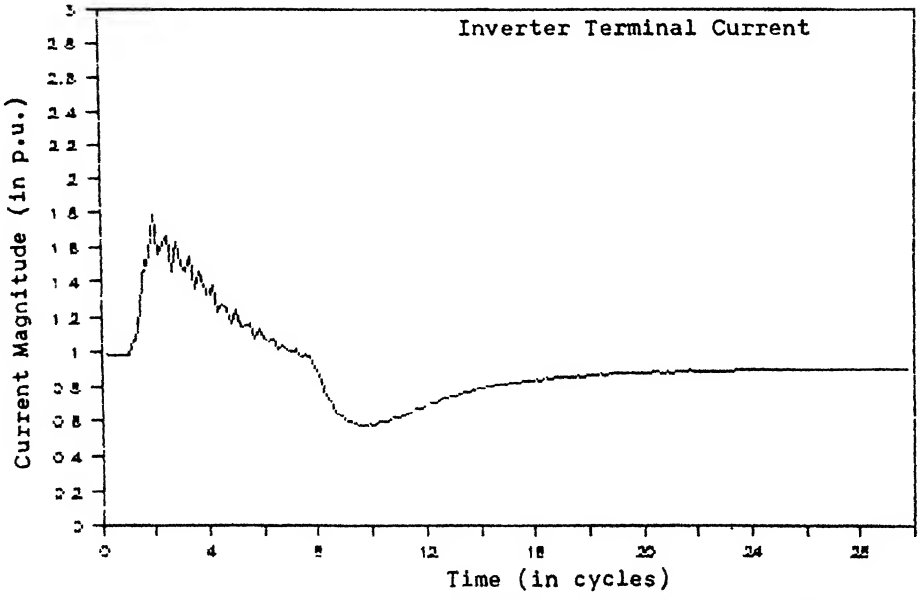




Fig. 4.5 50%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER
NORMAL RECOVERY



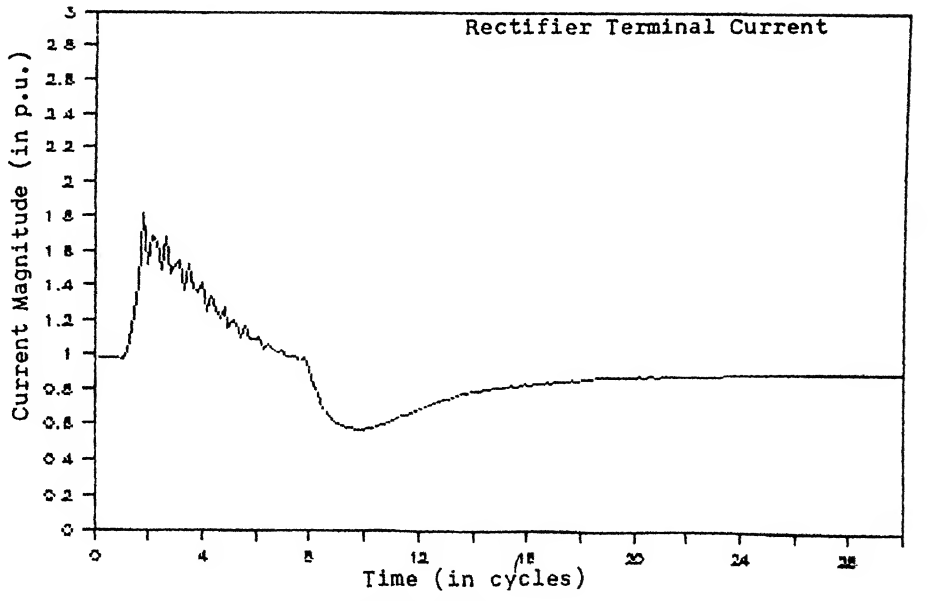
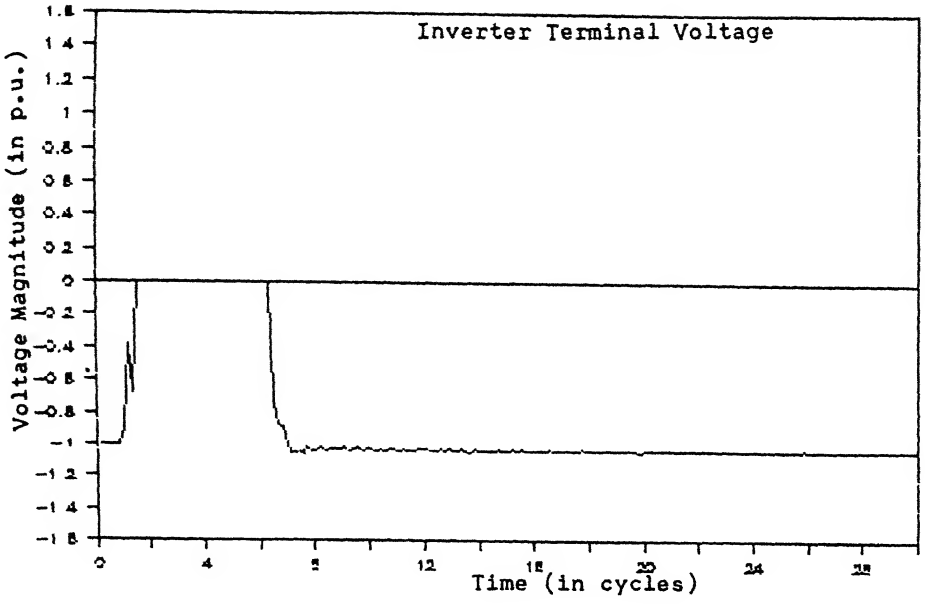
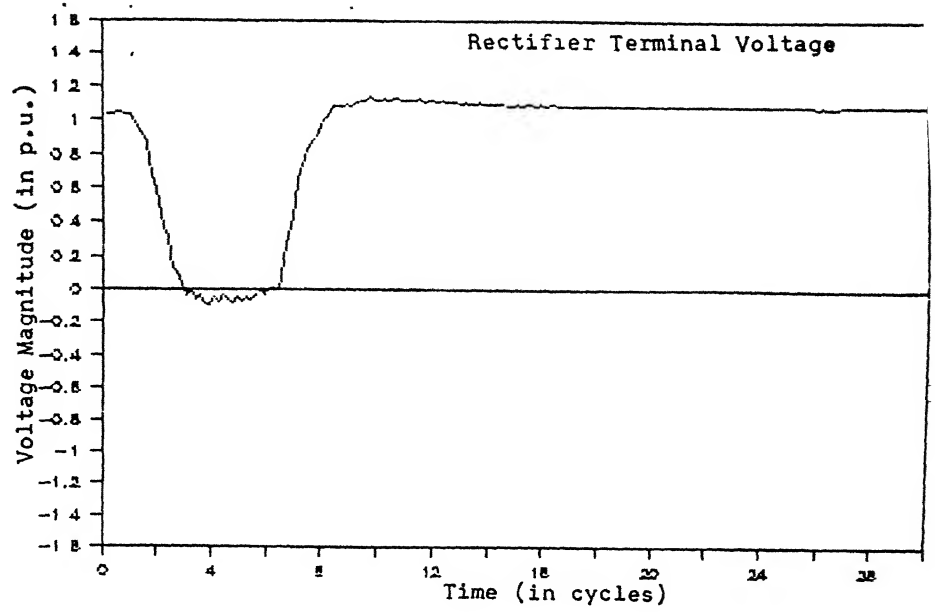
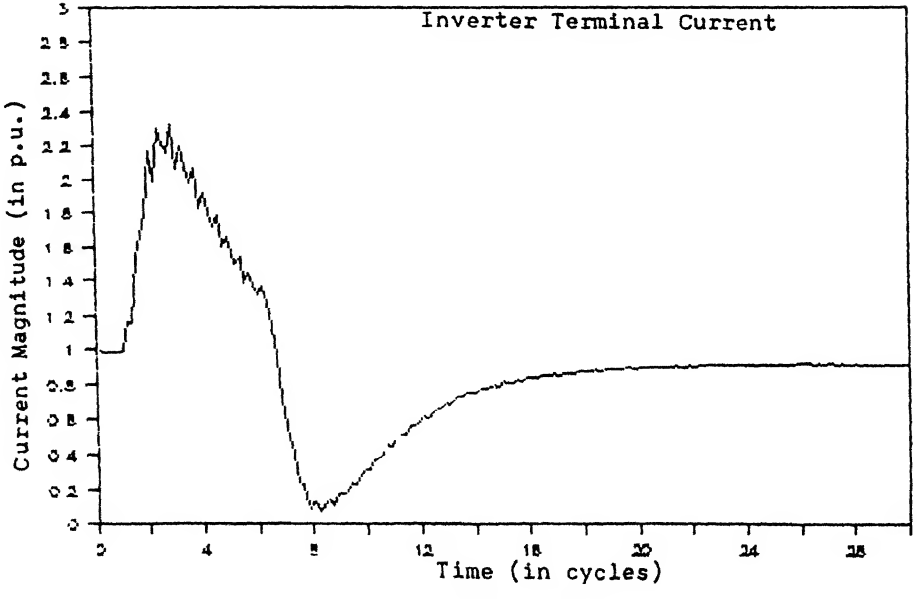




Fig. 4.6 50%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



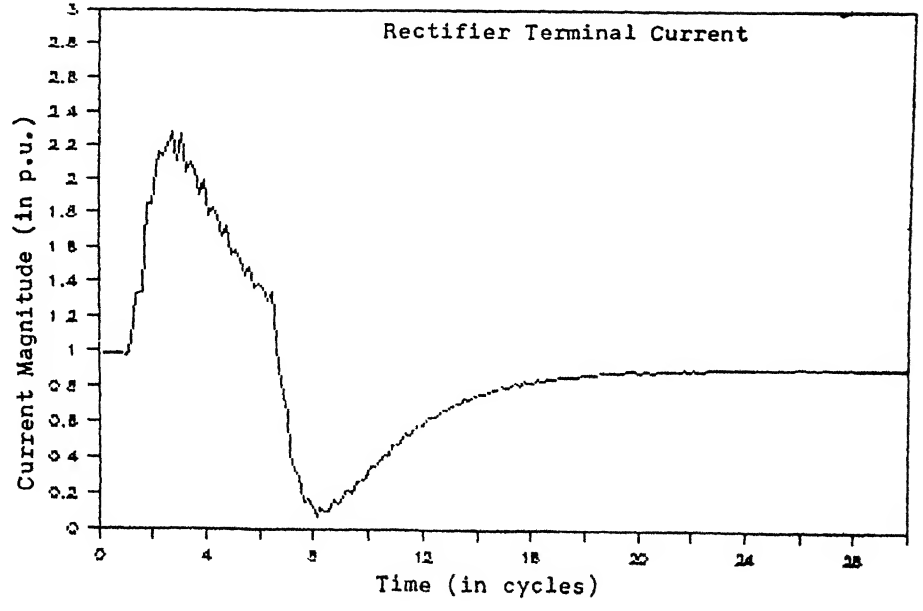
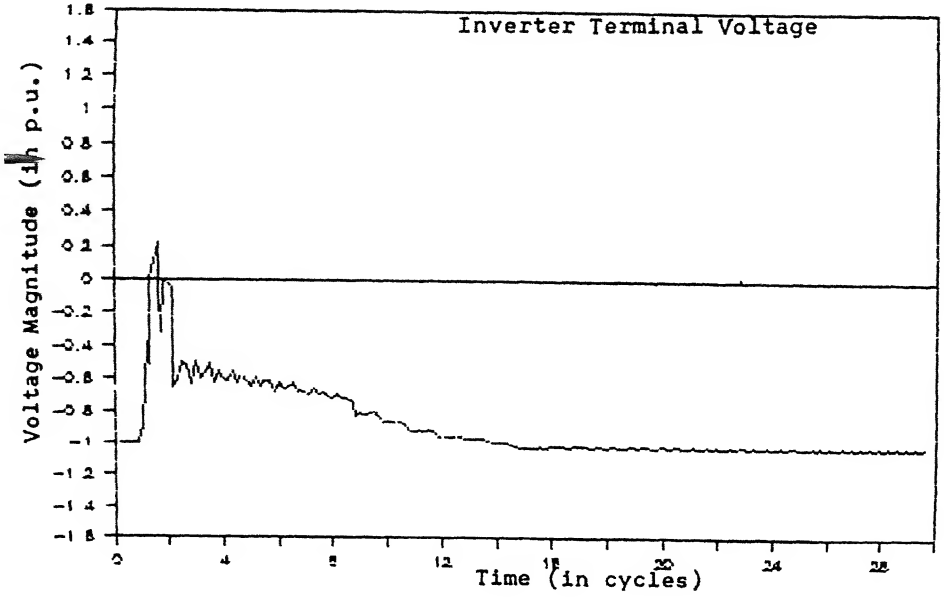
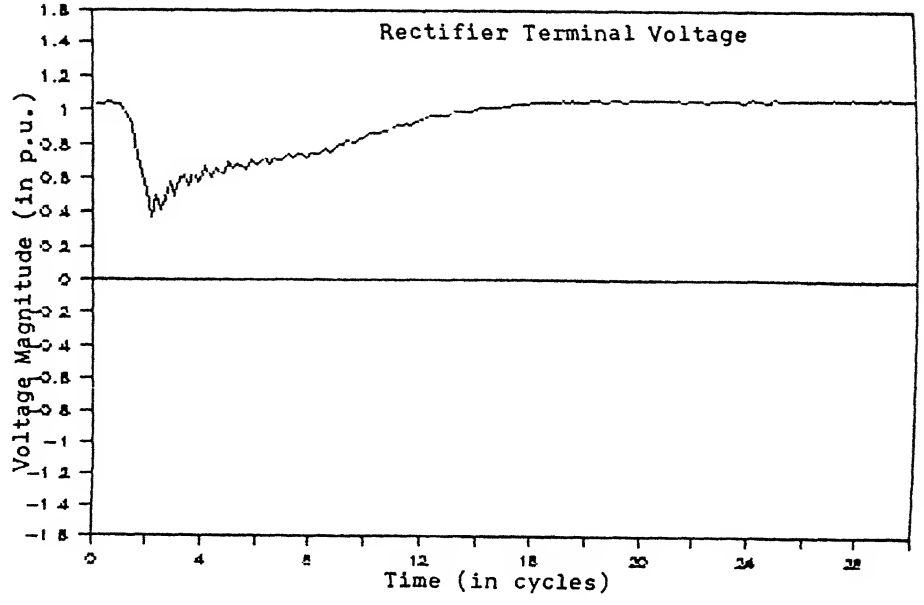
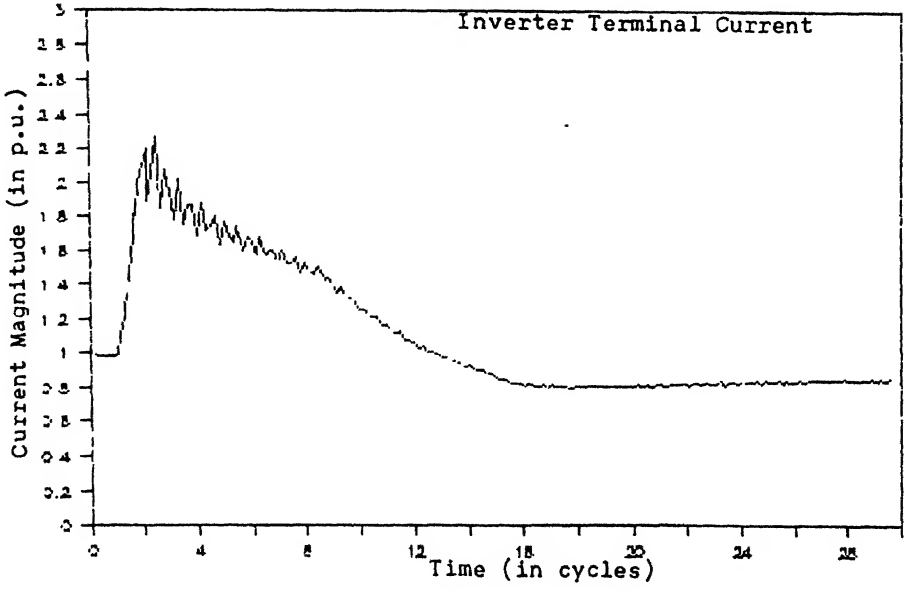




Fig. 4.7 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER
NORMAL RECOVERY



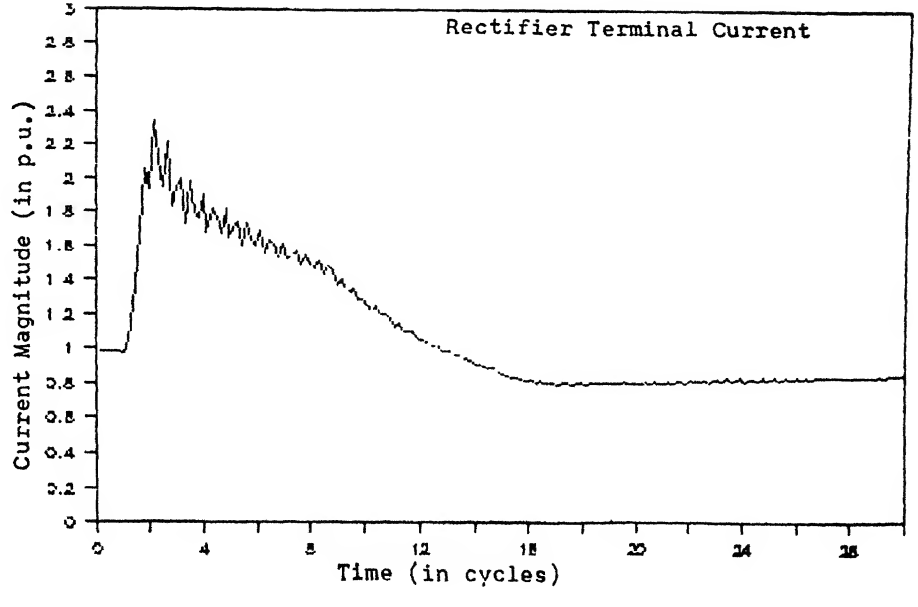




Fig. 4.8 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME

considerably by reducing the duration of the short circuit across the inverter terminal. However, the positive voltage at the inverter terminal for a short duration is the price for using the proposed scheme. The large variations in the rectifier terminal voltage and line current have been reduced to a great extent with the proposed recovery scheme. Overall, it can be concluded that the proposed recovery scheme is quite effective in case of single phase momentary faults.

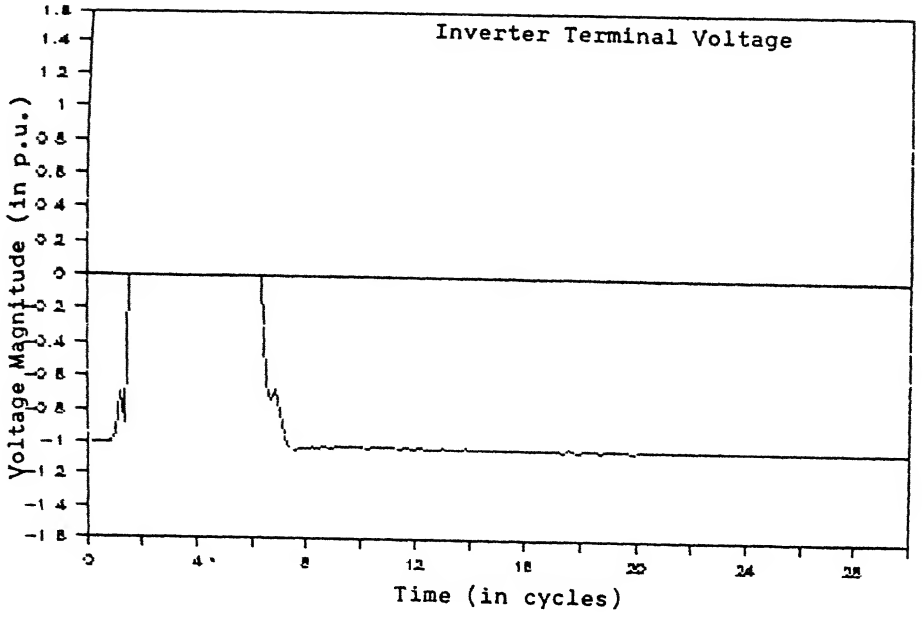
### 4.5.2 Prolonged Single Phase to Ground Faults

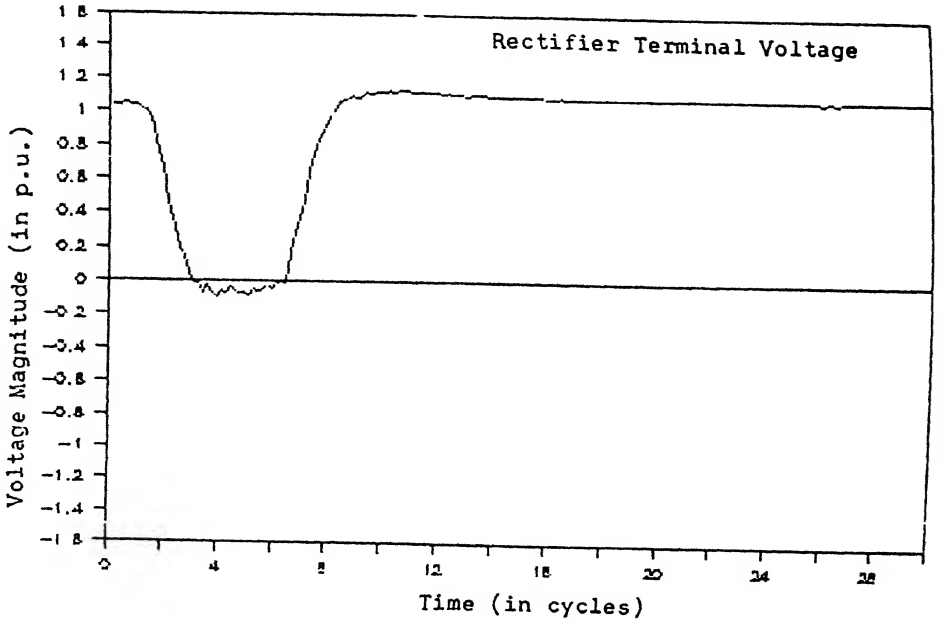
In this section following faults are considered :

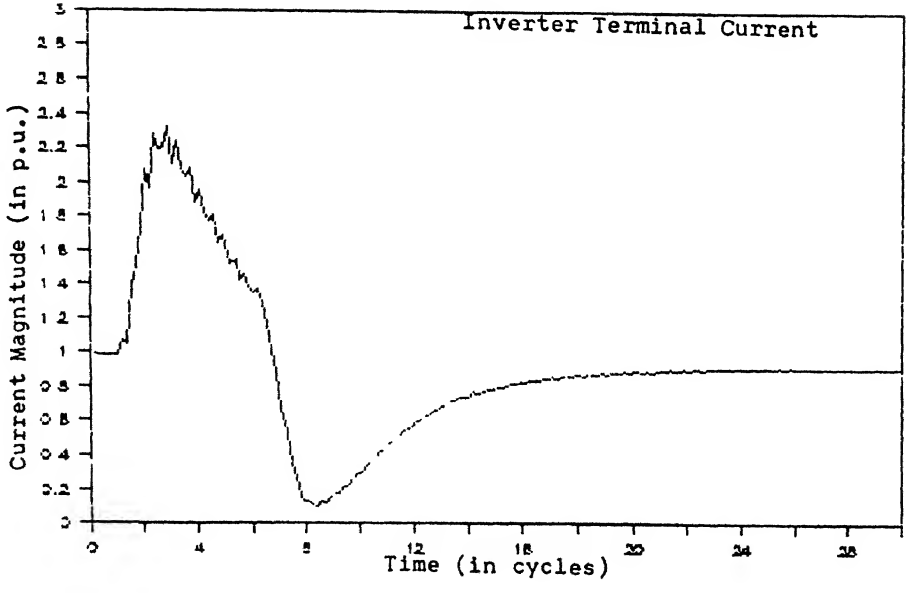
a) 5 cycle, 50% dip in phase A voltage

b) 5 cycle, 99% dip in phase A voltage

Figs. 4.9 and 4.10 show the system response for the fault in case A with the normal recovery and with the proposed recovery scheme respectively. It is evident from the Fig. 4.9 that short circuit across the inverter terminal persists for the whole duration of the fault. Whereas, with the proposed scheme the duration of the short circuit has been reduced considerably which consequently reduces the magnitude of the variations in rectifier terminal voltage and line current. Also it may be noticed that with the proposed scheme there is about 60% of rated power transfer over the line even during the fault . For a single phase to ground fault at inverter terminal for 5 cycles, the system response is reported in Figs. 4.11 and



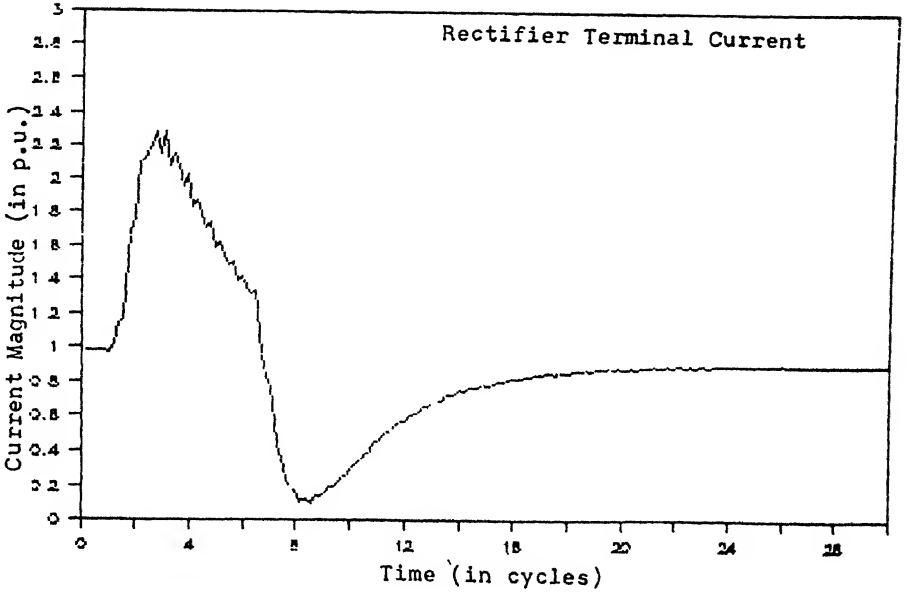
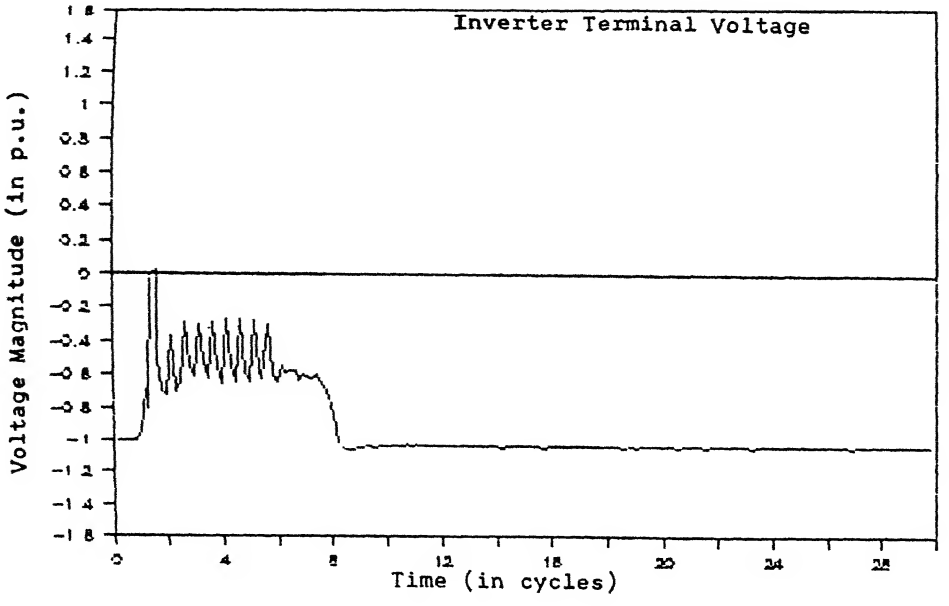
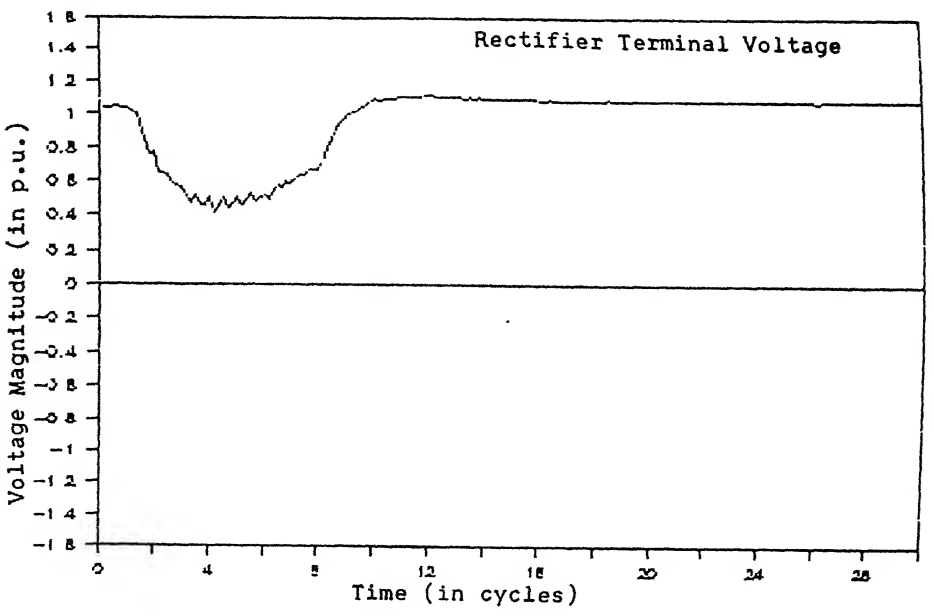
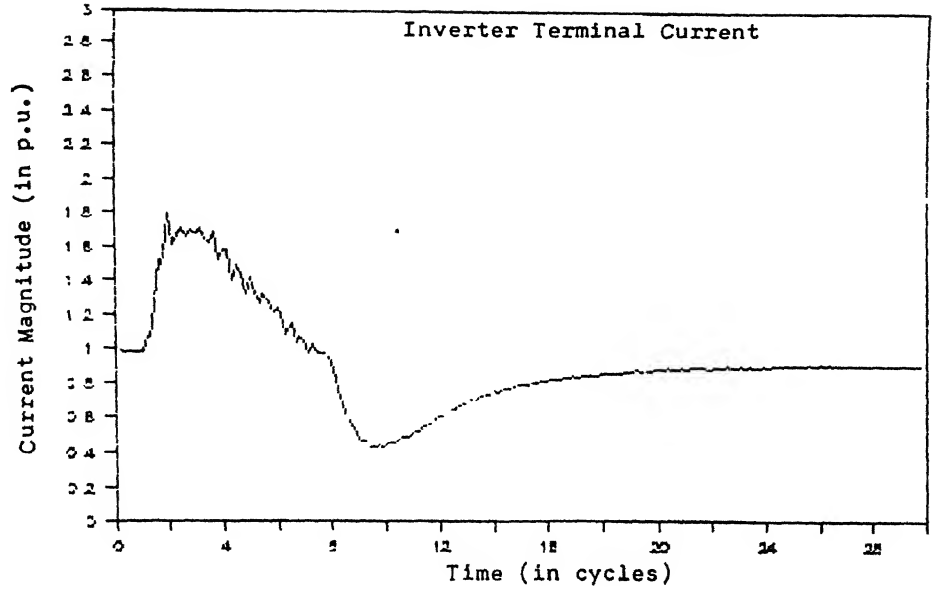




Fig. 4.9 50%, SINGLE PHASE, 5 CYCLE DIP AT INVERTER
NORMAL RECOVERY



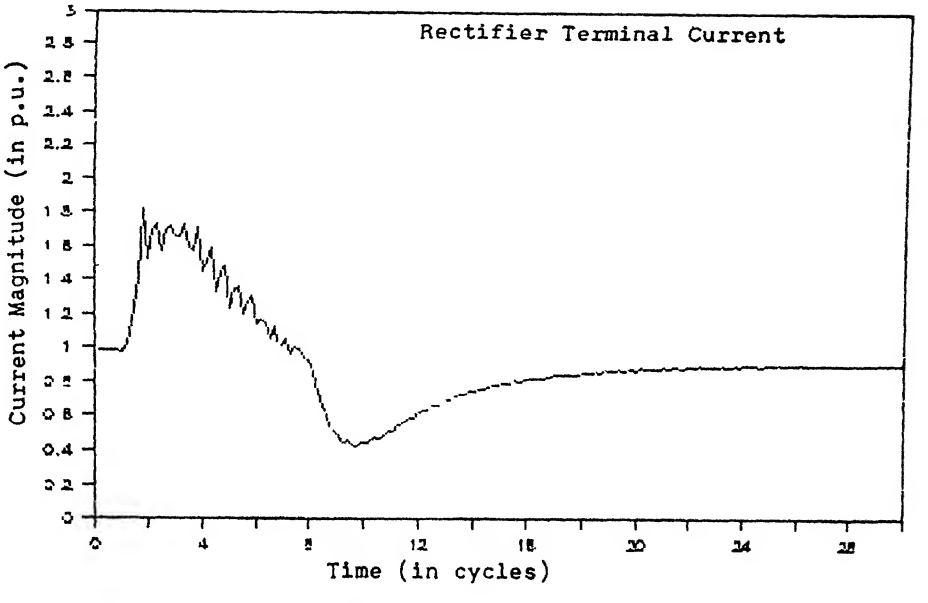
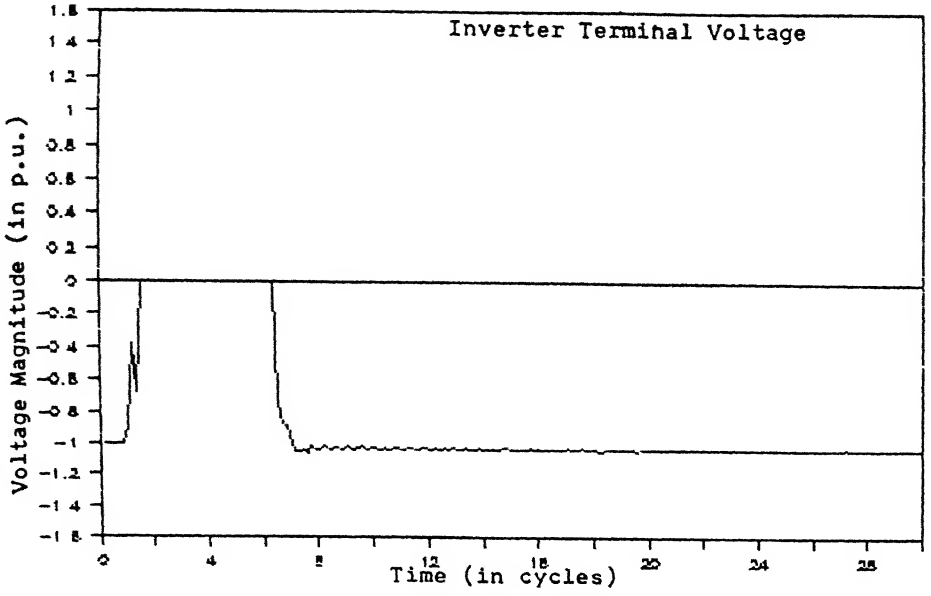
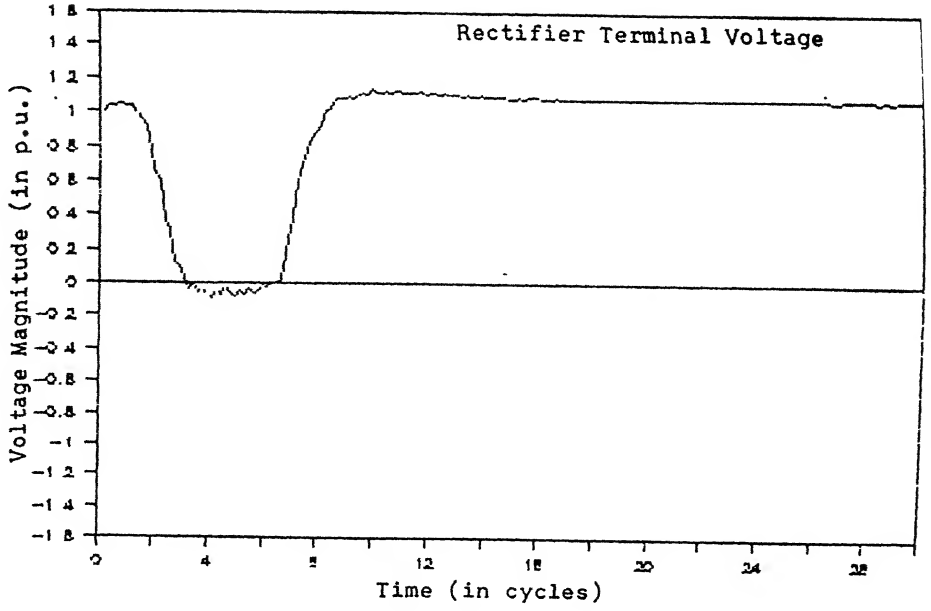
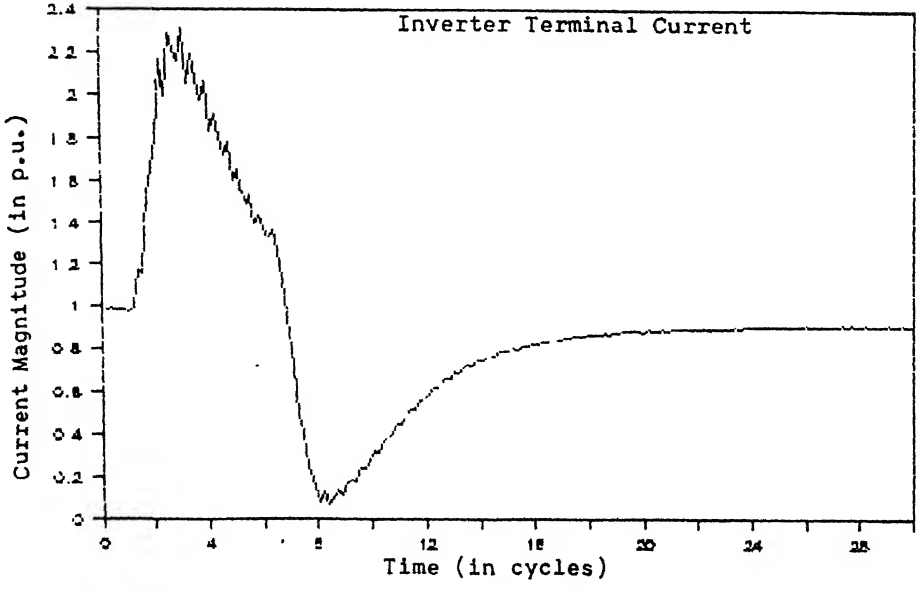




Fig. 4.10 50%, SINGLE PHASE, 5 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



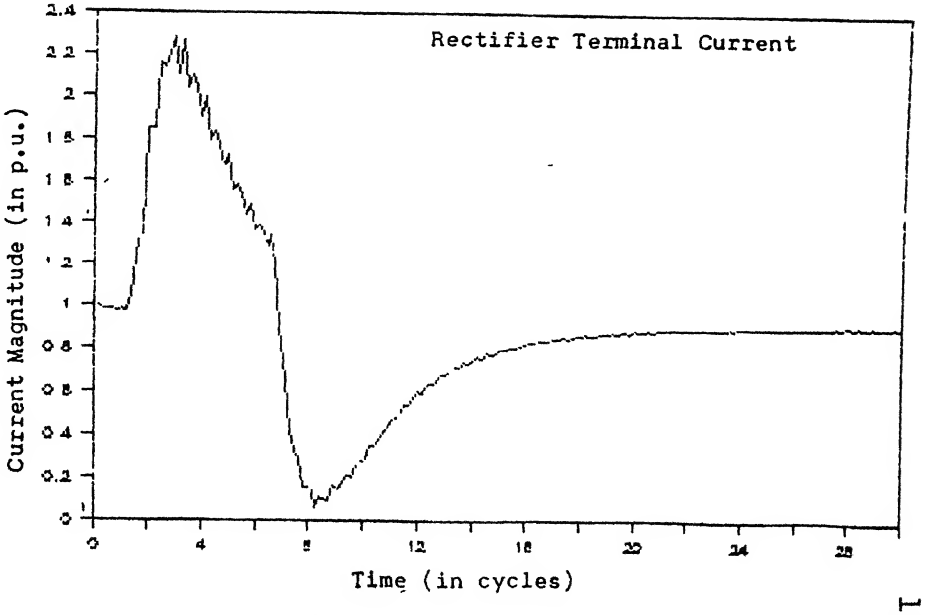
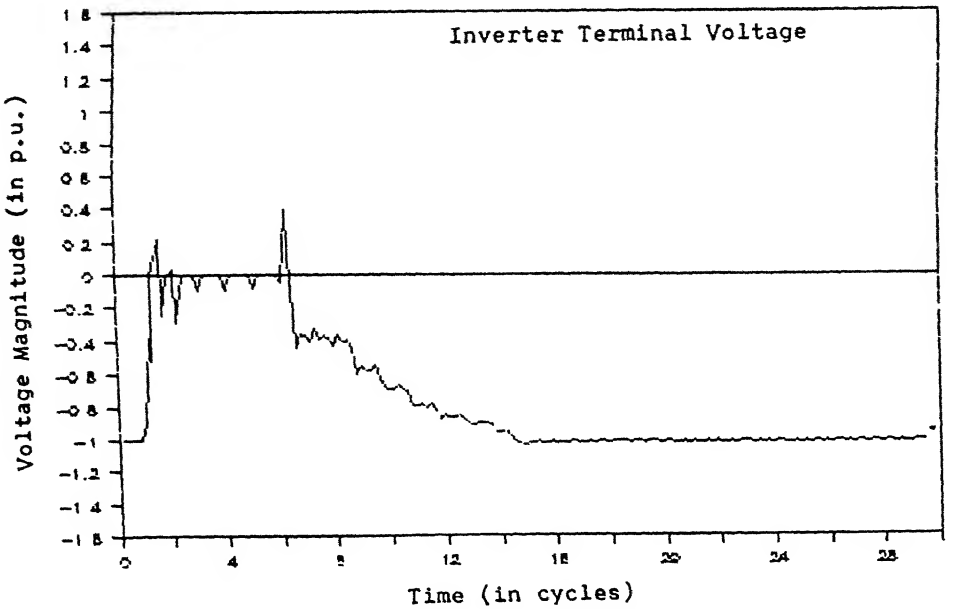
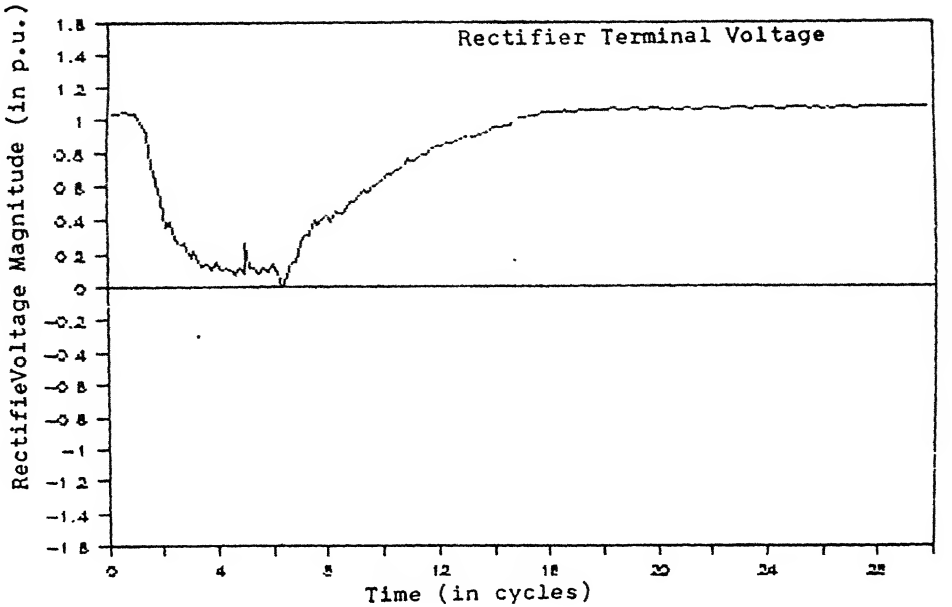
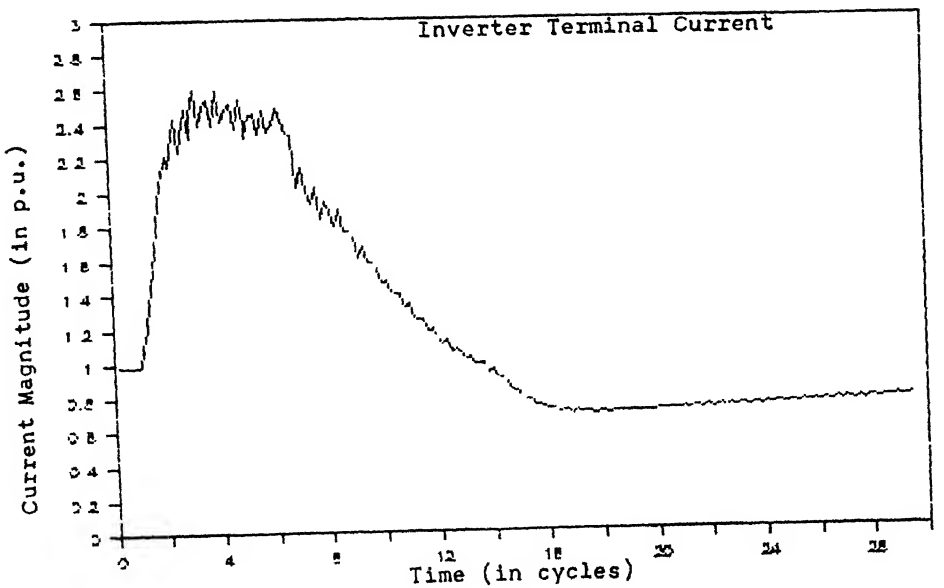




Fig. 4.11 99%, SINGLE PHASE, 5 CYCLE DIP AT INVERTER
NORMAL RECOVERY



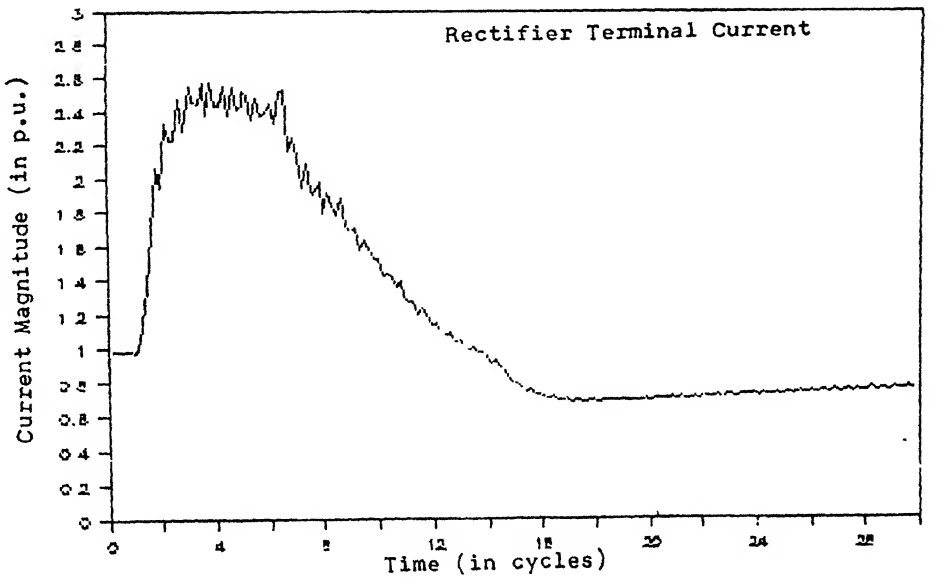




Fig. 4.12 99%, SINGLE PHASE, 5 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME

4.12.With the normal recovery process, the inverter terminal remains short circuited for the whole duration of the fault leading to large variations in the rectifier terminal voltage and line current.With the proposed recovery scheme, inverter makes continuous attempts to commutate but fails to do so during the fault. However, slight improvement can be noticed in rectifier terminal voltage and line current with the proposed scheme.

### 4.5.3 3-Phase to Ground Faults

In this section following faults are considered :

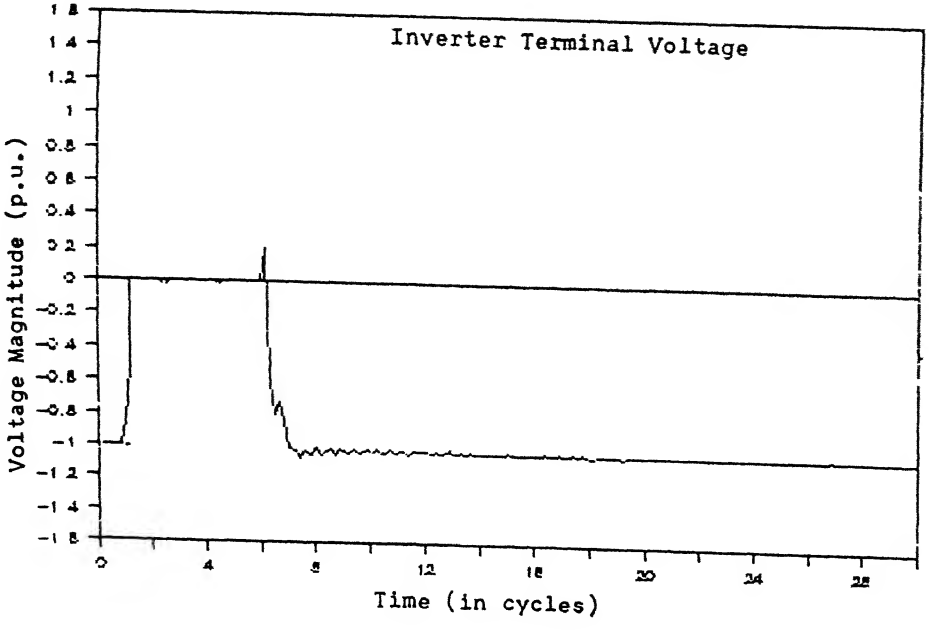
a) 5 cycle, 50% dip in all the three phases

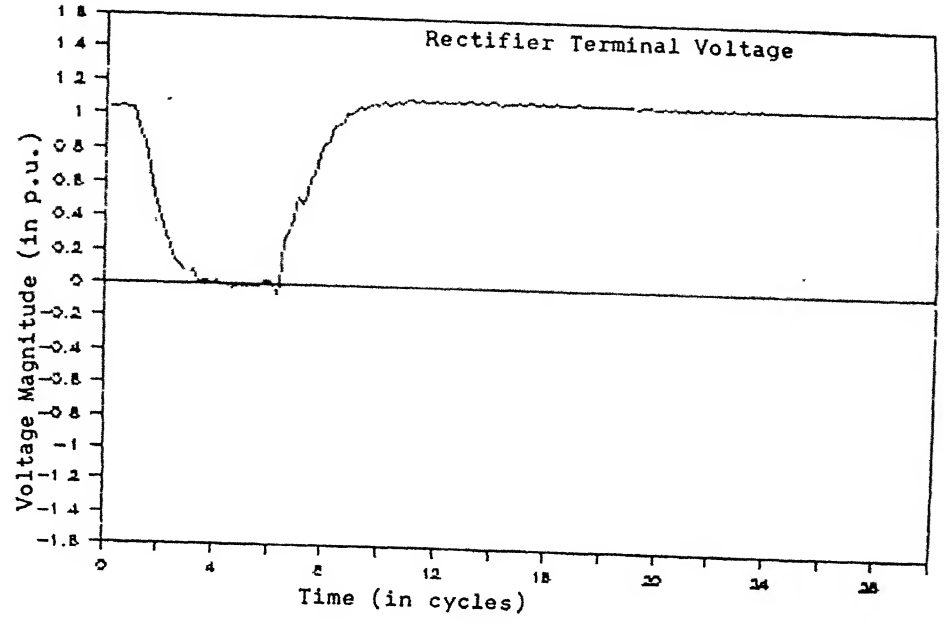
b) 5 cycle, 99% dip in all the three phases

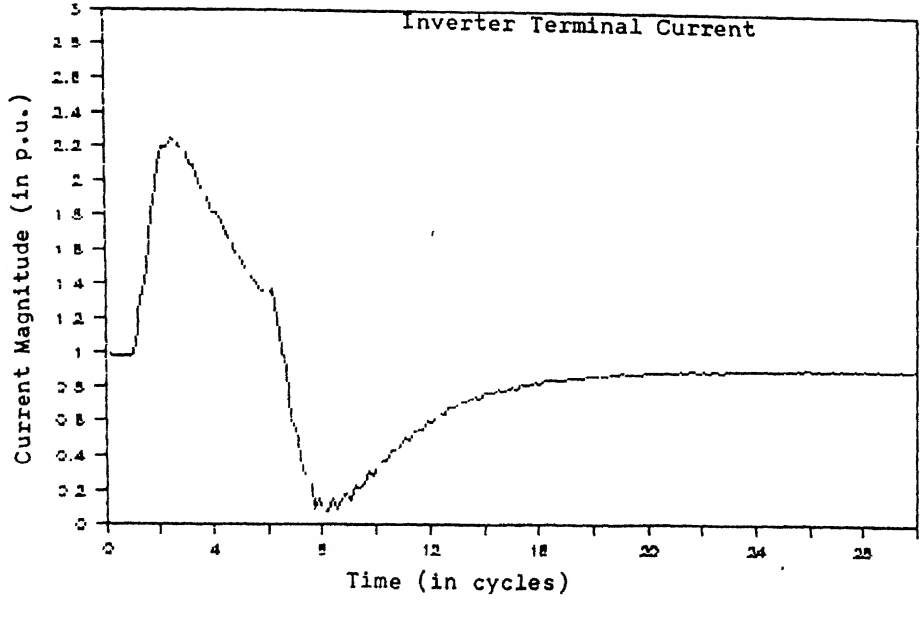
The system response for these faults is reported in Figs. 4.13 to 4.16. It can be seen from these figures that the system response under normal recovery and with the proposed scheme is not very much different. In fact the proposed scheme behaves more like a normal recovery during three phase disturbances. However, as reported earlier, the proposed scheme does improve the system response in the events of single phase disturbances.

## 4.6 CONCLUSIONS

This chapter is devoted to further validate the recovery scheme proposed in the previous chapter to improve the system



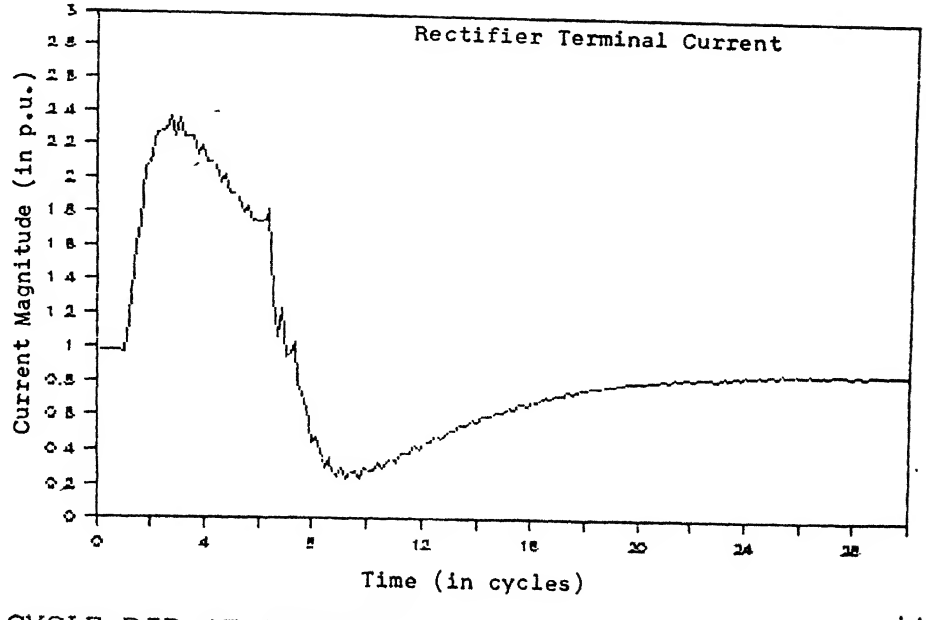
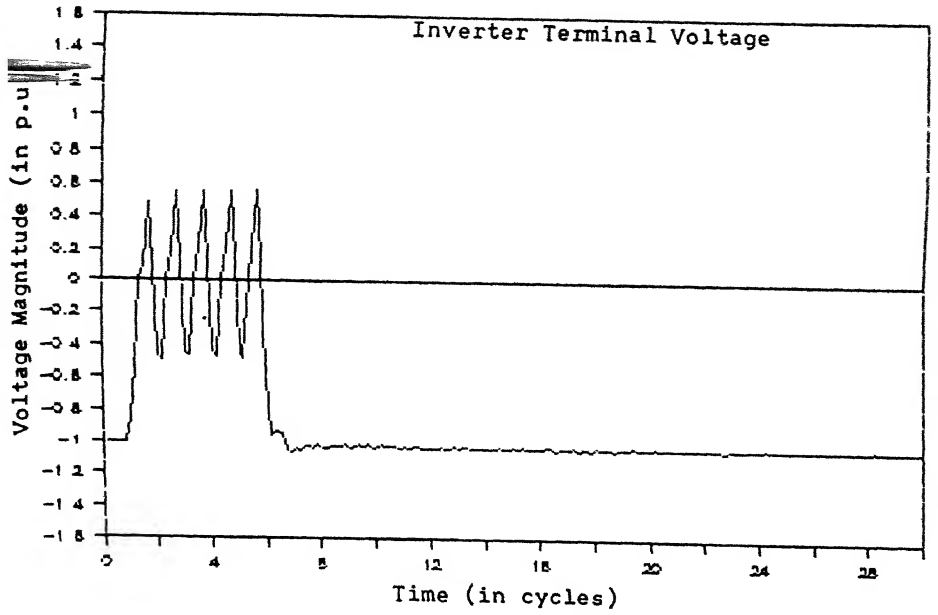
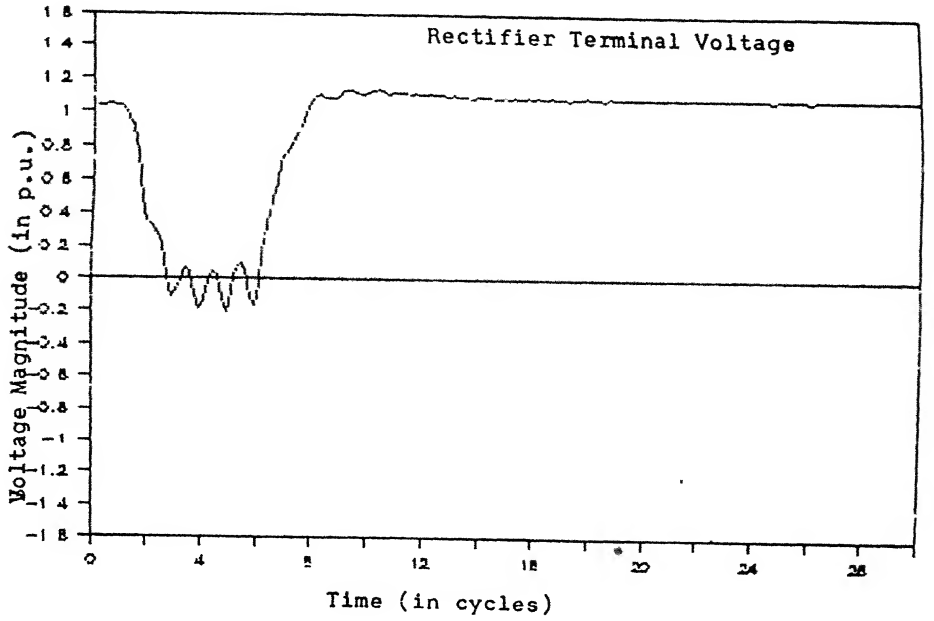
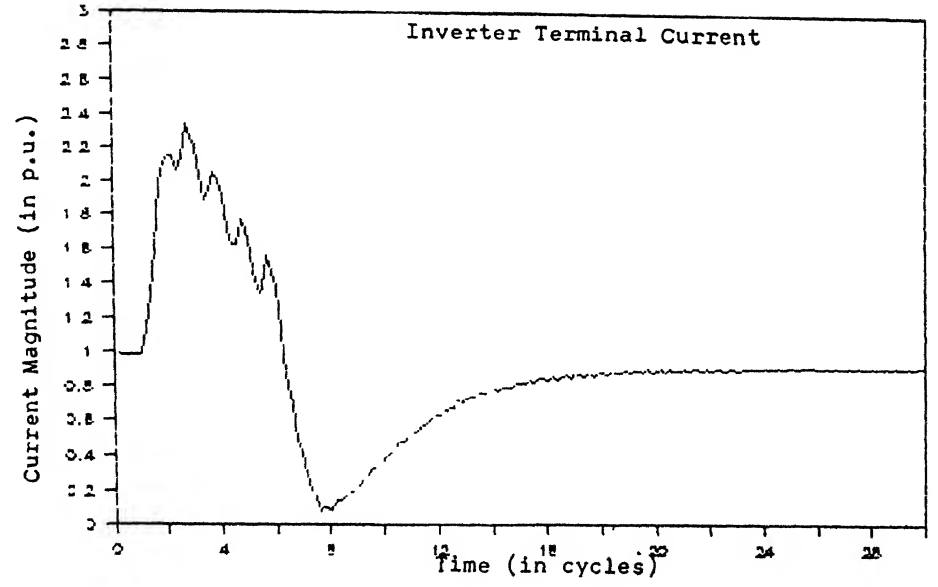




Fig. 4.13 50%, 3 PHASE, 5 CYCLE DIP AT INVERTER
NORMAL RECOVERY



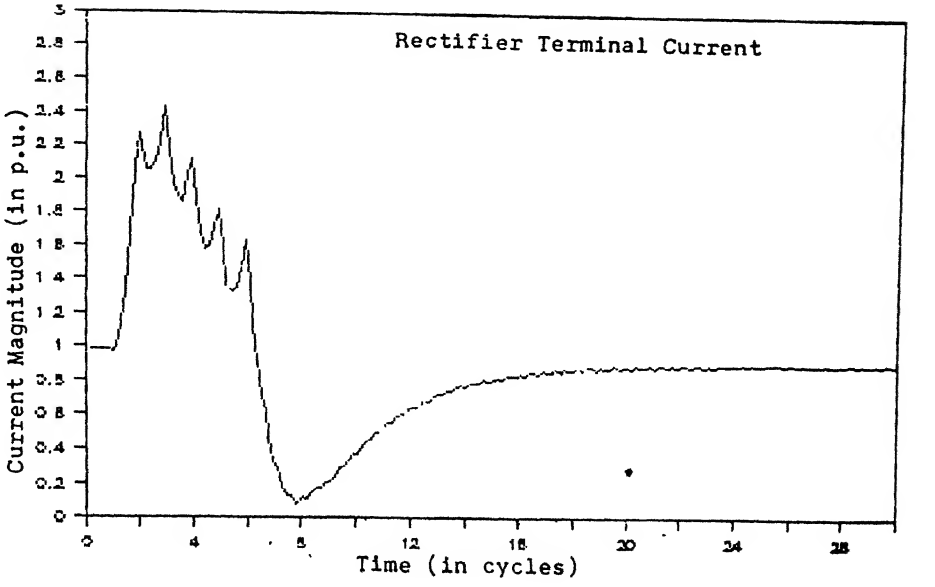
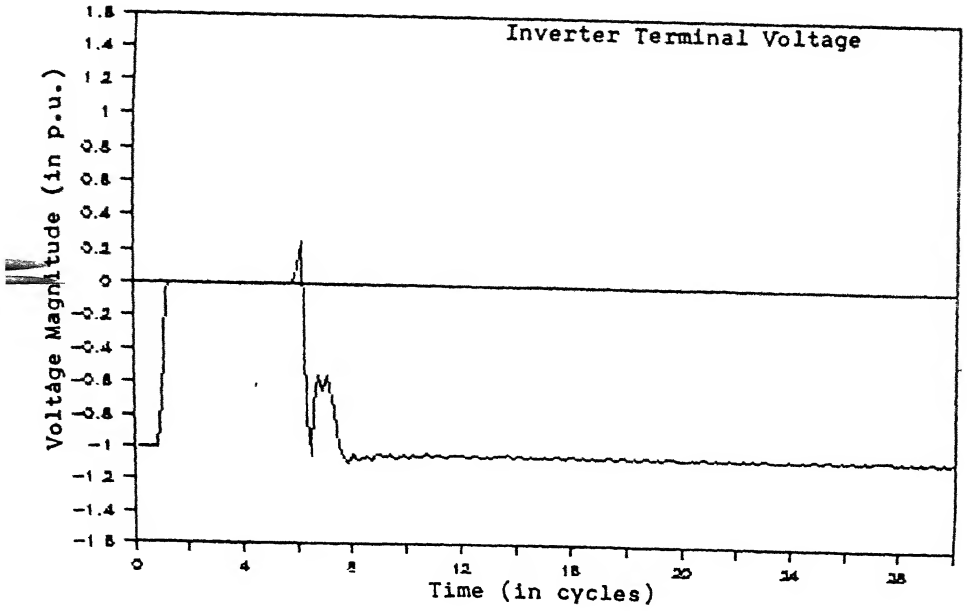
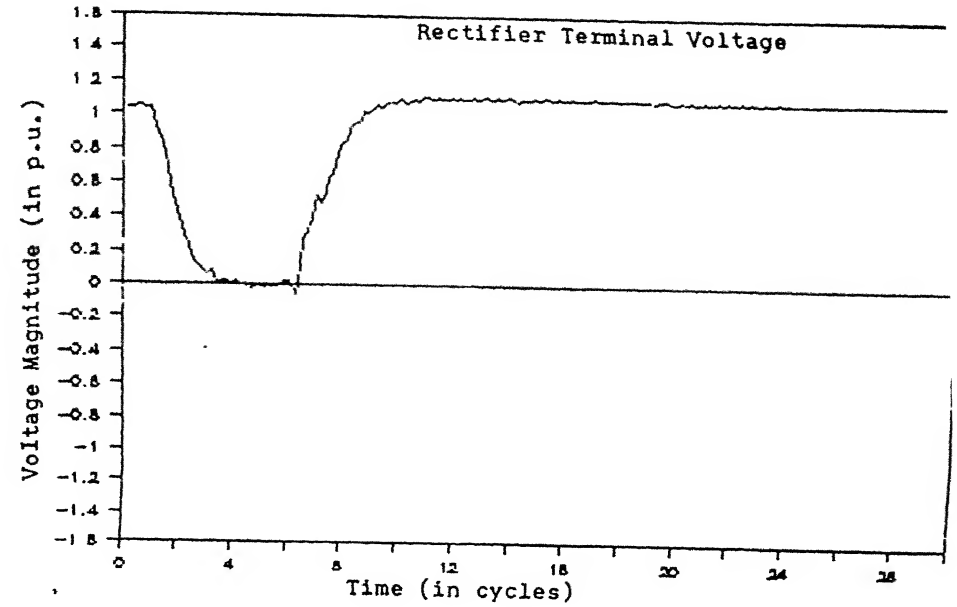
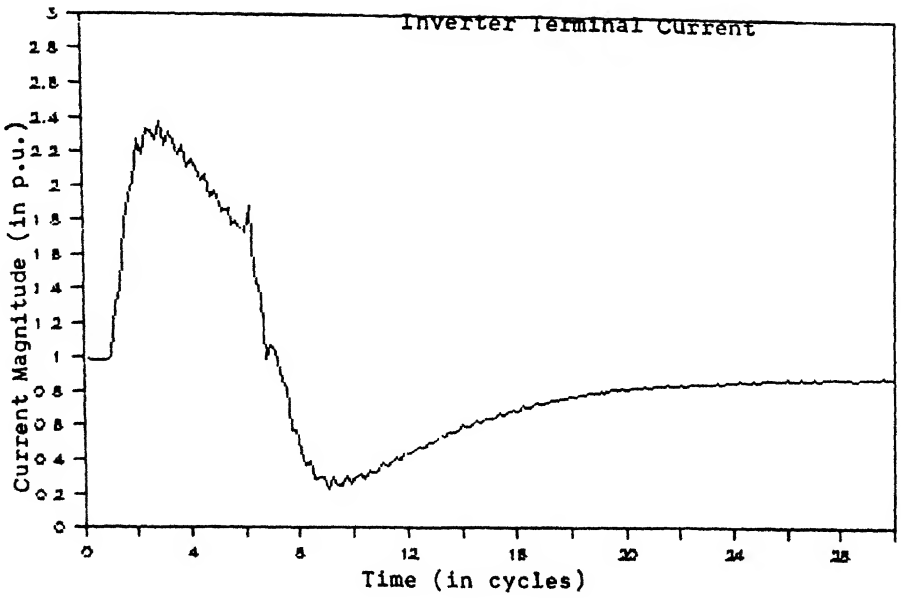




Fig. 4.14 50%, 3 PHASE, 5 CYCLE DIP AT INVERTER WITH THE PROPOSED SCHEME



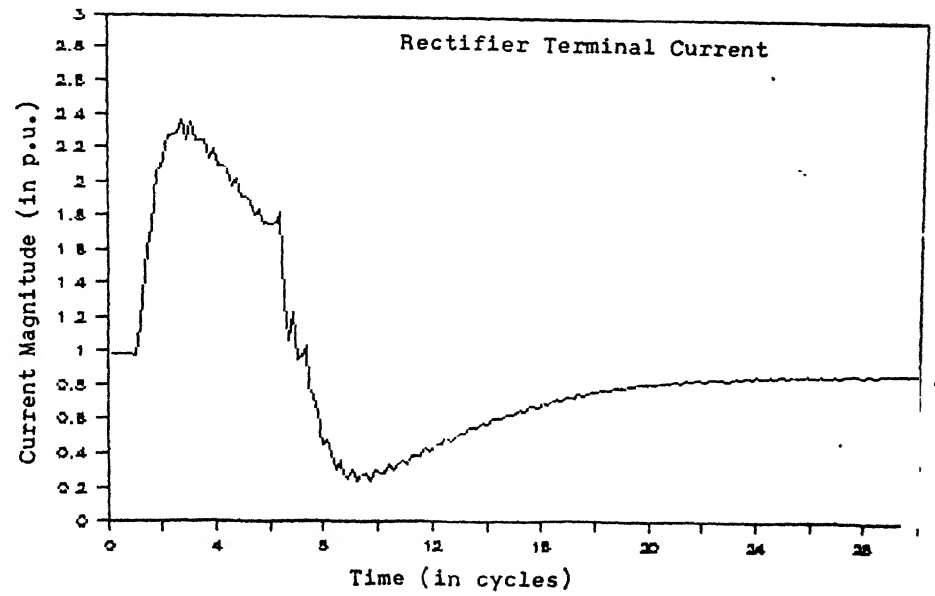
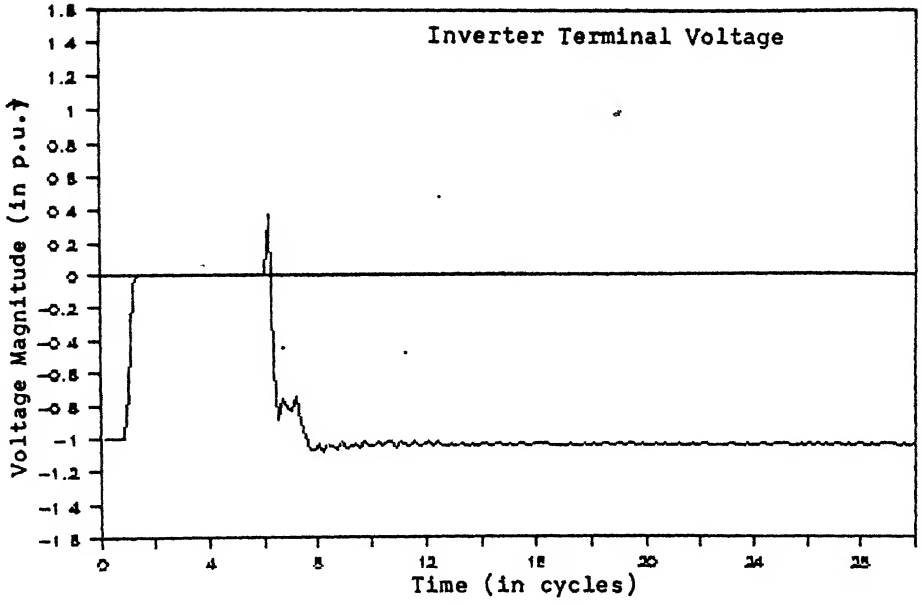
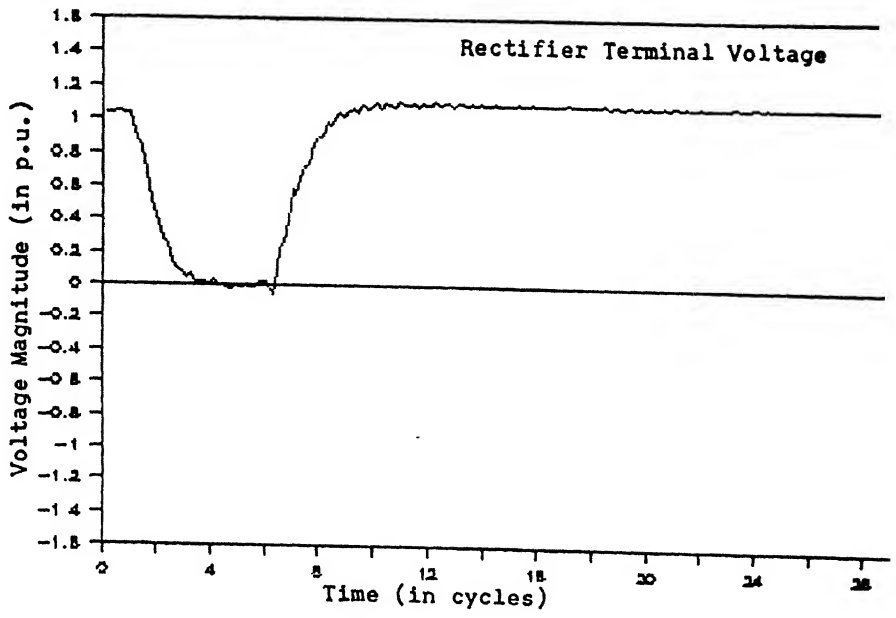
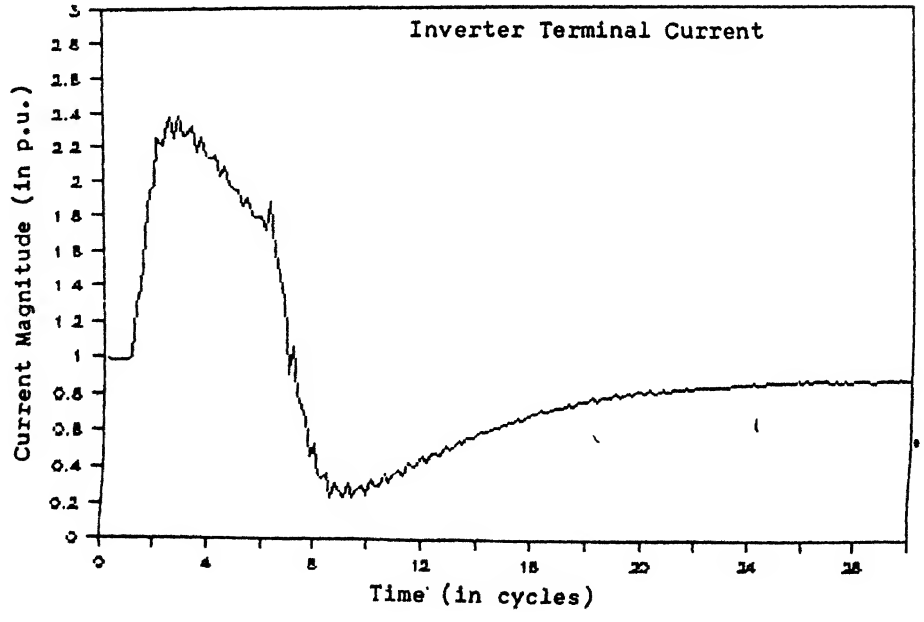




Fig. 4.15 99%, 3 PHASE, 5 CYCLE DIP AT INVERTER
NORMAL RECOVERY



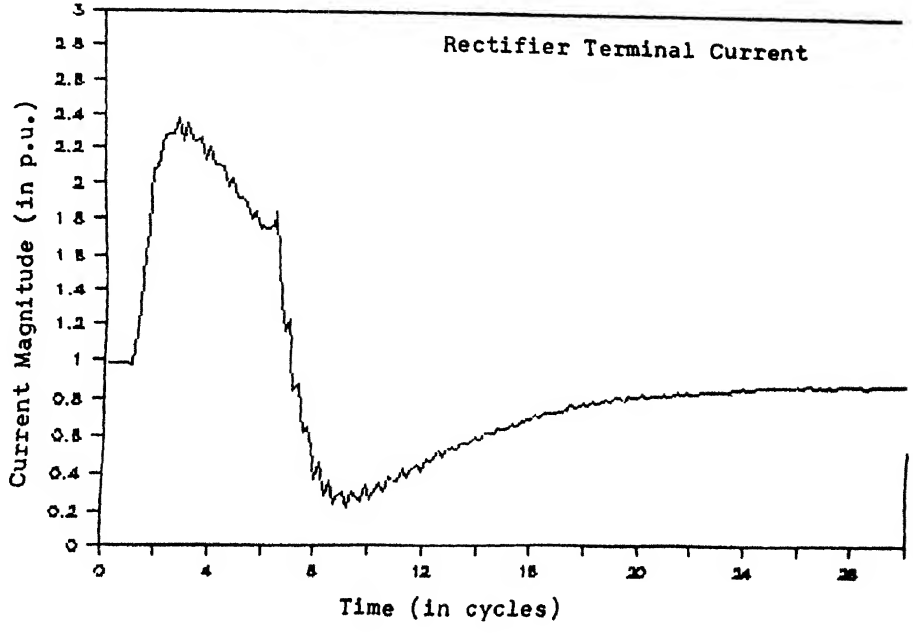




Fig. 4.16 99%, 3 PHASE, 5 CYCLE DIP AT INVERTER
WITH THE PROPOSED SCHEME

response following a commutation failure. The validity of the scheme is checked by studying the various cases considering different types of faults on the system of National HVDC experimental project. The results of the various case studies illustrate the effectiveness of the recovery scheme proposed.

# CHAPTER 5

## CONCLUSIONS

To ensure reliable and satisfactory operation of the HVDC system it is important that the control of the HVDC system should be effective under normal as well as abnormal operating conditions. Hence, for designing an effective control system, various abnormal situations arising in HVDC system must be taken care of. These abnormal operating conditions basically come because of the faults in DC or AC systems. The most frequent fault in AC system is single phase to ground fault which leads to the reduction in the magnitude of the AC phase voltages. The magnitude of the reduction depends on the location of the fault. If the dip in the magnitude of the AC phase voltages occurs at the bus where the HVDC converter (inverter in particular) is connected, it invariably leads to the commutation failure in the inverters. As a result, commutation failure is a very frequent fault in the inverters. Moreover, the behaviour of the inverter following some other faults/maloperations like misfire, arcquenching etc. is same as that following the commutation failure. Hence, it becomes quite important to study the behaviour of HVDC system during the and following the commutation failure.

In Chapter 2, an analysis of the inverter operation with unbalanced AC supply has been carried out to investigate the impact of unbalance on the commutation process. Although the unbalance in the AC supply may be because of the dip in more than one phases, only single phase dip is considered in the analysis. The analysis also takes into account the instant at which the dip occurs. Certain assumptions have been made to simplify the analysis which from the inverter operation point of view represent the worst situation. It is observed from the analysis that the commutation process is predominantly effected by the magnitude of the dip in the AC phase voltage. Also, the commutation failure occurs between the two valves only when the outgoing valve is connected to the phase which has undergone the voltage dip.

This conclusion has been validated also through digital simulation study of HVDC system. It is also observed that the main factor leading to commutation failure is the reduction in the time margin available for the commutation process. The reduction in the time margin is because of the dip in the AC phase voltages which leads to the shifting of the zero crossing of the commutation voltages. Hence, in order to avoid the further commutation failures the time margin available for the commutation process should be increased which can be done by advancing the firing of the succeeding valves.

Several techniques for advancing the firing has been reported in literature [5]. In Chapter 3, a scheme has been proposed to advance the firing based on the information of the commutation process. In the proposed scheme, if any commutation process is not complete before the instant where the commutation voltages of the two valves involved in the commutation process reverses, the next valve is fired immediately at that instant, thereby advancing its firing. Succeeding valves are also fired at specific instants in such a way so as to advance their firing. This helps system recover fast, also it is observed that if the firing of first valve after the imminent commutation failure is delayed, the system response deteriorates. This fact is examined by modifying the proposed scheme. The theoretical aspects of the scheme have been explained in detail and various cases considering different types of faults like remote short duration and prolonged faults, severe short duration and prolonged faults have been studied. Based upon the various cases studied it can be observed that the proposed scheme improves the system response following a commutation failure. However, the improvement is quite considerable in case of remote momentary and prolonged faults but is not so effective in case of severe prolonged and 3 phase faults. It is also noticed that in the cases where the scheme is not very effective, it does not hamper the recovery process. Chapter 4

is basically devoted to further validate the effectiveness of the proposed scheme by studying the various faults. On the system of National HVDC experimental project.From the results of the various cases studied it is evident that the response of the system following the commutation failure has improved considerably with the proposed recovery scheme thereby validating the results obtained in Chapter 3.

## 5.1 FUTURE SCOPE OF THE WORK

1) The conver analysis has been carried out considering unbalance only in the single phase. This should be extended to study the effect of unbalance in more than one phases.

2) The commutation process between two valves fails only when the outgoing valve is connected to the phase which has experienced the dip. If the dip occurs at a certain instant there may be some time available before the commutation process which is susceptible to failure begins. It may be interesting to examine some firing strategy during this time interval so as to minimise the impact of disturbance.

3) The effect of advancing the firing, based on the proposed scheme, on the converter reactive power requirement should be studied in detail.

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3. Ajai Srivastava, 'Study of HVDC System with Digital Control Scheme', M.Tech. Thesis, IIT Kanpur, May, 1987.
4. A. Ekstrom and G. Liss, 'A Refined HVDC Control System', IEEE Transactions on Power Apparatus and Systems, vol. 89, May/June 1970, pp 723-732.
5. J. Arrillaga and G. Galanos, 'Theoretical basis of a digital method of Grid Control for HVDC converters', IEEE Transactions on Power Apparatus and Systems, vol. 89, Nov/Dec. 1970, pp 2049-2055.
6. J. Reeve and J.A. Sevcenco, 'An Automatic Control Scheme for HVDC Transmission Using Digital Techniques - Part I - Principles of Operation, Part 2 - Circuit Considerations and Performance', IEEE Transactions on Power Apparatus and Systems, vol. 91, 1972, pp 2319-2332.
7. Subroto Bhattacharya, 'Digital Simulation of 12 pulse Converter', M.Tech. Thesis, I.I.T. Kanpur, August 1983.
8. J. Arrillaga, 'High Voltage Direct Current Transmission'.
9. Personal Communication with BHEL.

# APPENDIX A

## SYSTEM DATA (adapted from reference [7])

DC base voltage = 100 kV

DC base current = 1 kV

DC base impedance = 100 Ohms

Rated Power of DC Link = 240 MW for 12 pulse system

= 120 MW for 6 pulse system

AC system frequency = 50 Hz

Bridge Transformer :

Resistance $R_{c1} = R_{c2}$ = 0.5 Ohms

Commutating Reactance $X_{c1} = X_{c2}$ = 6.283 Ohms

Smoothing Reactor :

Resistance $R_{d1} = R_{d2}$ = 0.1 Ohms

Reactance $X_{d1} = X_{d2}$ = 314.159 Ohms

Transmission Line :

Total resistance = 8.64 Ohms

Total inductance = 0.50148 H

Total capacitance = 54.1645 μF

Any number of PI sections upto a maximum of 10 may be specified.

Digital Controller (adapted from reference [10])

a) Constant Current Controller

$K_1$ = 0.4 radians/per unit current

$K_2$ = 0.4 radians$^2$/per unit current

b) Constant Extinction Angle Controller

$K_3 = 1.0$

$K_4 = 0.25$

RMS AC Voltages (L-N)

$E_1 = 42.78$ kV, $E_2 = 38.51$ kV

Valve turn off time = $3^\circ$

Operating conditions :

a) 12 pulse :

$I_{d1} = I_{d2} = 1000$ Amps

$\alpha_{min} = 5^\circ$, $\gamma_c = 10^\circ$

$\alpha_1 = 26.22^\circ$, $\alpha_2 = 148.39^\circ$

b) 6 pulse :

$I_{d1} = I_{d2} = 1000$ Amps

$\alpha_{min} = 5^\circ$, $\gamma_c = 10^\circ$

$\alpha_1 = 12.88^\circ$, $\alpha_2 = 148.38^\circ$

DC Filter parameters :

$R = 0.096$ p.u.

$L_1 = 0.20267$ p.u.

$L_2 = 0.5947411$ p.u.

$C_1 = 0.047183$ p.u.

$C_2 = 0.136659$ p.u.

AC Filter Configuration :

AC Filter Parameters

| Harmonic No. | Resistance Ohms | Inductance mH | Capacitance μF |
|---|---|---|---|
| 5 | 1.11418 | 36.32860 | 11.1346 |
| 7 | 0.801103 | 18.16430 | 11.13748 |
| 11 | 0.504805 | 7.26573 | 11.5102 |
| 13 | 0.4225 | 5.20478 | 11.5331 |
| HP | 16.1428 | 3.00410 | 11.5791 |

VDCOL Parameters :

6 Pulse Operation

a) At Rectifier

$T_{DN}$ = 0.00008 sec; $T_{UP}$ = 0.03 sec

Corner points :

| | | | |
|---|---|---|---|
| Voltage (p.u.): | 0.6 | 0.2 | 0.0 |
| Current (p.u.): | 1.0 | 0.4 | 0.4 |

b) At Inverter

$T_{DN}$ = 0.00008 sec; $T_{UP}$ = 0.04 sec

Corner points :

| | | | |
|---|---|---|---|
| Voltage (p.u.): | 0.6 | 0.2 | 0.0 |
| Current (p.u.): | 0.9 | 0.3 | 0.3 |

12 Pulse Operation

a) At Rectifier

$T_{DN}$ = 0.00008 sec; $T_{UP}$ = 0.03 sec

Corner points :

| | | | |
|---|---|---|---|
| Voltage (p.u.): | 1.2 | 0.4 | 0.0 |
| Current (p.u.): | 1.0 | 0.4 | 0.4 |

b) At Inverter

$T_{DN}$ = 0.00008 sec; $T_{UP}$ = 0.04 sec

Corner points :

| | | | |
|---|---|---|---|
| Voltage (p.u.): | 1.2 | 0.4 | 0.0 |
| Current (p.u.): | 0.9 | 0.3 | 0.3 |

# APPENDIX B

## SYSTEM DATA FOR NATIONAL HVDC EXPERIMENTAL PROJECT

National HVDC project is an experimental DC line between Lower Sileru in A.P. and Barsoor in M.P. The line is 196 km long. The project comprises of 6 pulse monopole HVDC system.

DC base voltage = 100 kV

DC base current = 1 kA

DC base impedance = 100 Ohms

Rated power of dc link = 100 MW

Rated voltage of dc link = 1 kV

AC system frequency = 50 Hz

Bridge Transformer :

3 single phase transformers

$X_c$ = 19.5% on 40.5 MVA Base

Rating 220/86.6 kV

Inductance of the transformer = 0.038318 H

Transformer resistance is neglected

Smoothing Reactor :

Resistance of the smoothing reactor is neglected

Inductance = 0.45 H

Transmission line :

Total resistance = 5.2 Ohms (lumped)

Total inductance = 0.08 H (lumped)

Total capacitance = 5.37 μF

Transmission line is represented by one 1 PI section

Control System.

a) Constant Current Controller

At Rectifier

$K_R$ = 0.18 rad/p.u. of current

$T_R$ = 46 ms

High switching gain used when I exceeds certain value.

$K_R$ = 8.8 rad/p.u. of current (However the value of D is not specified in data given so I = 0.25 p.u. is considered in Chapter 4)

At Inverter

$G_I$ = 0.13 rad/p.u. of current

$T_R$ = 60 ns

b) Constant Extinction Angle Controller

Gain of the controller = 1.0

RMS AC voltages (L-N)

$E_1$ = 51.781904 kV, $E_2$ = 51.899 kV

Valve turn off = $3^\circ$

Operating conditions

$I_{d1} = I_{d2}$ = 1000 Amps

$\alpha_{min} = 10^\circ$, $\alpha_{max} = 90^\circ$

$_c = 20^\circ$

$\alpha_1 = 16^\circ$, $\alpha_2 = 136.95^\circ$

DC filter parameters

R = 12.77 Ohms

$L_1$ = 1.0053 p.u.

$L_2$ = 0.3685 p.u.

$C_1$ = 0.02827 p.u.

$C_2$ = 0.01885 p.u.

VDCOL Parameters

a) At Rectifier

$T_{DN}$ = 4.7 ms , $T_{UP}$ = 47 ms

Corner points :

| | | | | |
|---|---|---|---|---|
| Voltage (p.u.): | 1.0 | 0.3 | 0.3 | 0.0 |
| Current (p.u.): | 1.0 | 1.0 | 0.3 | 0.3 |

b) At Inverter

$T_{DN}$ = 4.7 ms, $T_{UP}$ = 47 ms

Corner points for constant Beta characteristic

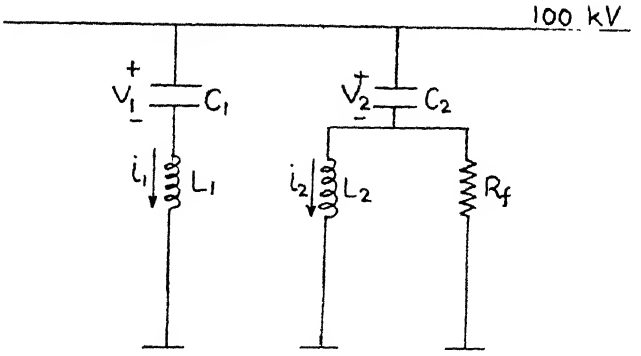
| | | |
|---|---|---|
| Voltage (p.u.) | 1.0 | 0.95 |
| Current (p.u.) | 1.0 | 0.90 |

Corner points for constant current characteristic

| | | | |
|---|---|---|---|
| Voltage (p.u.) | 6.5 | 0.4 | 0.0 |
| Current (p.u.) | 0.9 | 0.2 | 0.2 |

# APPENDIX C

## DC FILTER CONFIGURATION IN NHVDC SYSTEM




The capacitor voltage and inductor currents are taken as state variables.

The network equations are :

$$C_1 \frac{dV_1}{dt} = i_1$$

$$L_1 \frac{di_1}{dt} = V_{dc} - V_1$$

$$L_2 \frac{di_2}{dt} = V_{dc} - V_2$$

$$C_2 \frac{dV_2}{dt} = i_2 + (V_{dc}-V_2)/R_f$$

Hence the state equations are :

$$d/dt\ V_1 = i_1/C_1$$

$$d/dt\ V_2 = (i_2 + (V_{dc}-V_2)/R_f)/C_2$$

$$d/dt\ i_1 = (V_{dc}-V_1)/L_1$$

$$d/dt\ i_2 = (V_{dc}-V_2)/L_2$$

Initial conditions from DC solution are

$$V_1 = V_2 = V_{dc}\ ;\quad i_1 = i_2 = 0$$